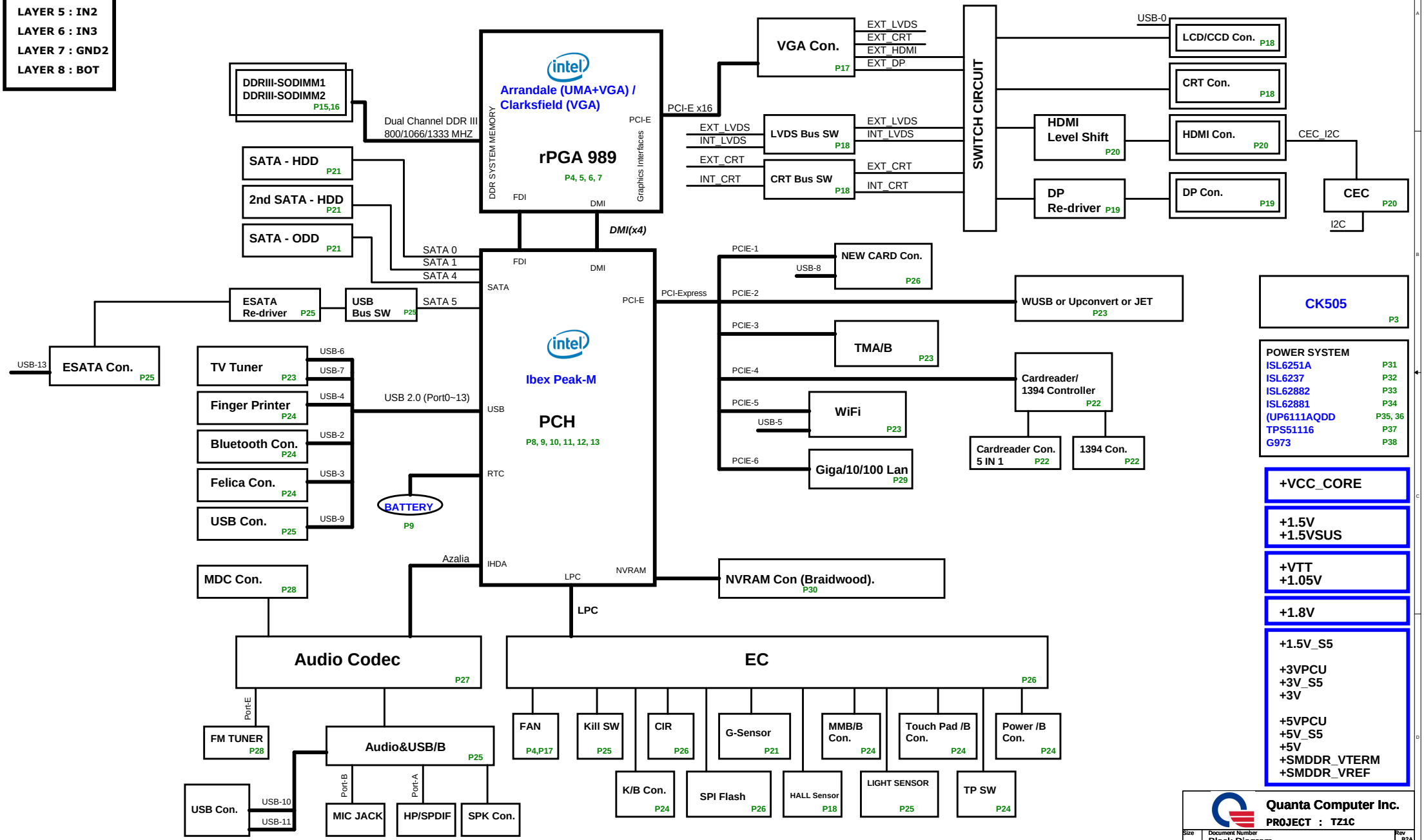
TZ1C Block Diagram

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : GND1
- LAYER 3 : IN1
- LAYER 4 : VCC
- LAYER 5 : IN2
- LAYER 6 : IN3
- LAYER 7 : GND2
- LAYER 8 : BOT



Quanta Computer Inc.
PROJECT : TZ1C

Size	Document Number	Rev
	Block Diagram	B2A

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Table of Contents

POWER PLANE	VOLTAGE	CONTROL SIGNAL	Power States ACTIVE IN
VIN	10V~+19V		S0~S5
+VCCRTC	+3.0V~+3.3V		S0~S5
+3V	+3.3V	MAIN_ON	S0
+3V_S5	+3.3V	S5_ON	S0~S5
+3V_HDP	+3.3V	MAIN_ON	S0
+3VPCU	+3.3V	AC/DC Insert enable	S0
+5V	+5V	MAIN_ON	S0
+5V_S5	+5V	S5_ON	S0~S5
+5VPCU	+5V	AC/DC Insert enable	S0~S5
+5V_TMA	+5V	MAIN_ON	S0
WIMAX_P	+3.3V	WMAX_P for EC	
+1.8V	+1.8V	MAIN_ON	S0
+1.5V	+1.5V	MAIN_ON	S0
+1.5V_S5	+1.5V	S5_ON	S0~S5
+1.5V_SUS	+1.5V	SUSON	S0~S3
+VCC_CORE		VRON	S0
+VTT	+1.05V~+1.1V	MAIN_ON	S0
+1.05V	+1.05V	MAIN_ON	S0
+VAXG		GFXVR_EN	S0

GND PLANE	PAGE
GND_SIGNAL	32
CARD_GND	21
AGND_DC/DC	31
GND	ALL

Quanta Computer Inc.

PROJECT : TZ1C

Size	Document Number	Rev
	FRONTPAGE	B2A

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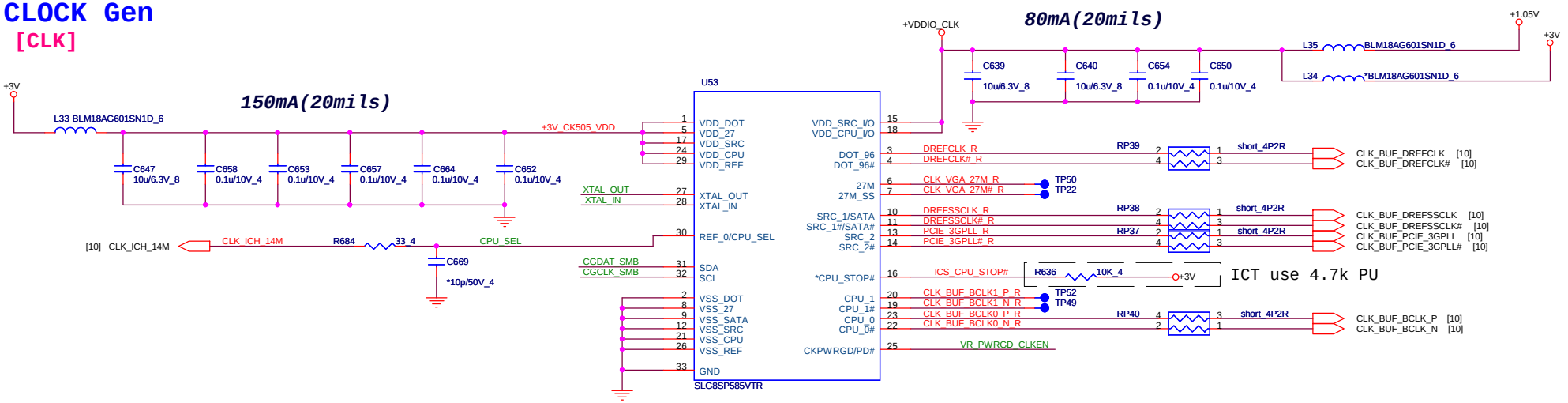
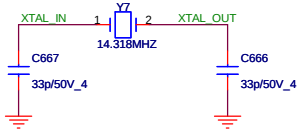
CLOCK Gen
[CLK]

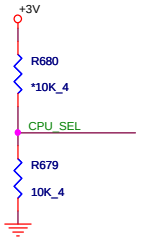
3



CLK CRYSTAL

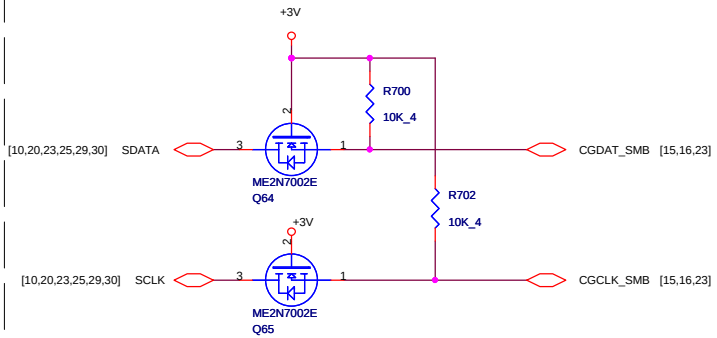


CLK CPU_SEL



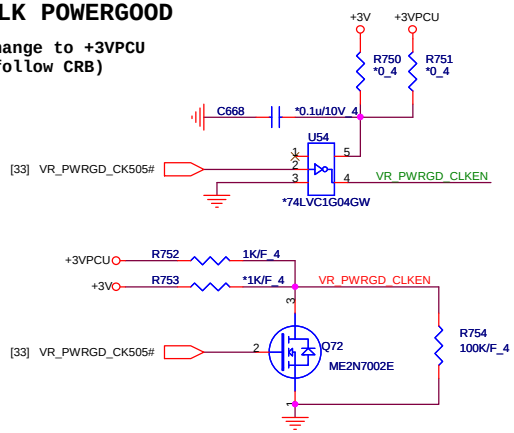
	0	1
CPU_SEL	CPU =133MHz (default)	CPU=100MHz

CLK I2C



CLK POWERGOOD

Change to +3VPCU
(follow CRB)



Quanta Computer Inc.
PROJECT : TZ1C

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	CLOCK GENERATOR	B2A
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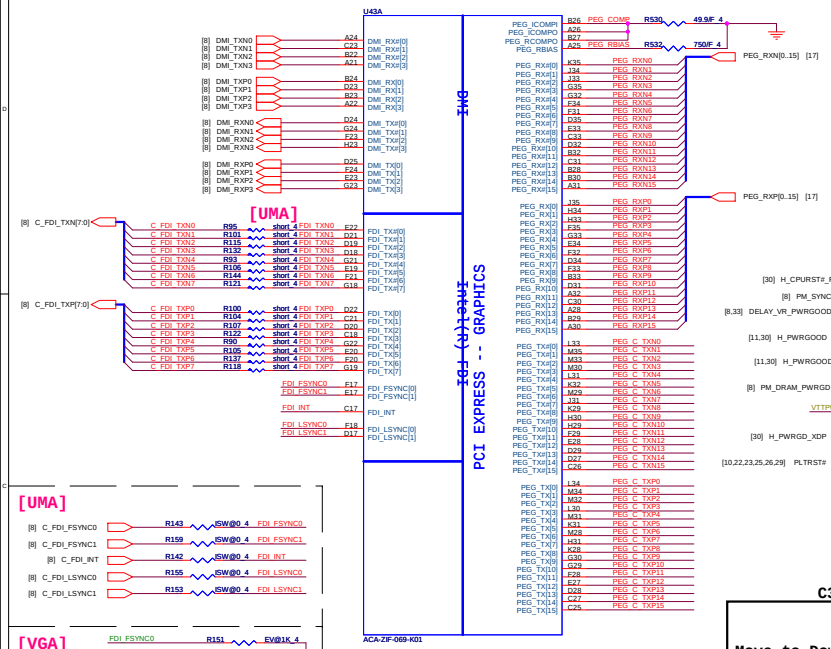
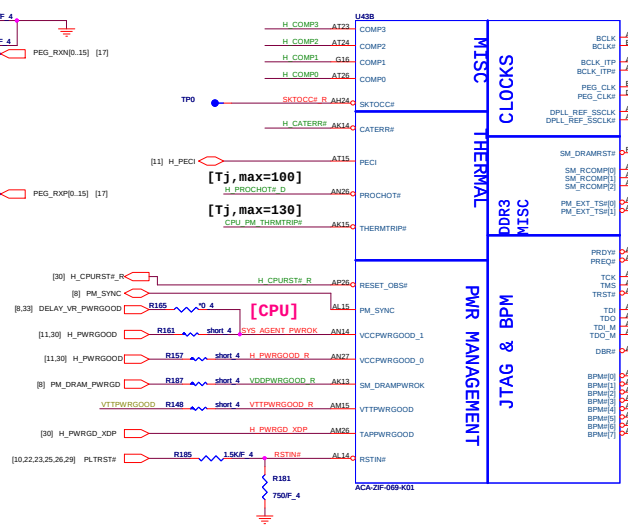
[CPU]

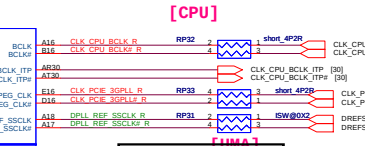
AUBURNDALE/CLARKSFIELD PROCESSOR (DMI,PEG,FDI)

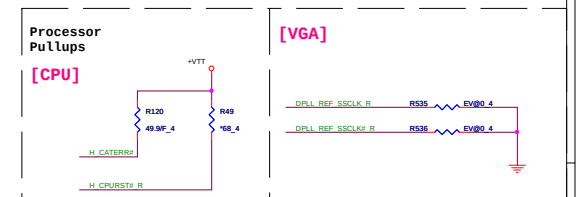
AUBURNDALE/CLARKSFIELD PROCESSOR (CLK,MISC,JTAG)

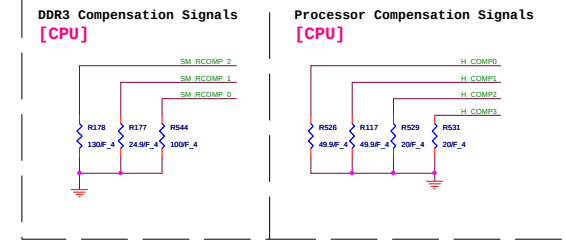
4

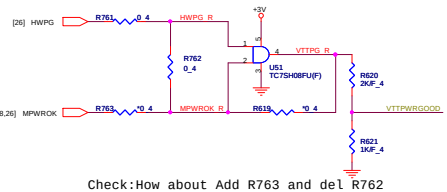








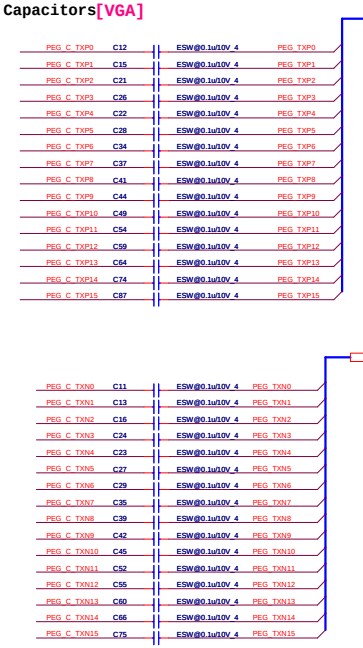




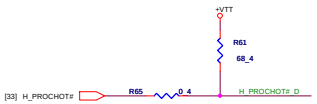
JTAG MAPPING [CPU]

Scan Chain (Default)	STUFF -> R58, R41, R29 NO STUFF -> R31, R53
CPU Only	STUFF -> R58, R31 NO STUFF -> R41, R53, R29
GMCH Only	STUFF -> R53, R29 NO STUFF -> R58, R31, R41

PEG AC Coupling Capacitors [VGA]

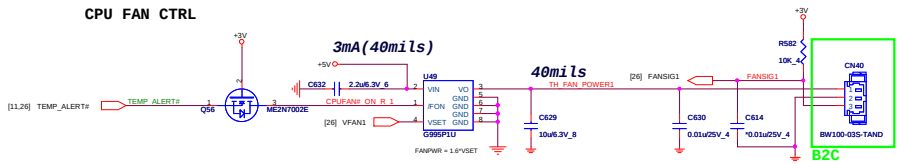


Processor hot

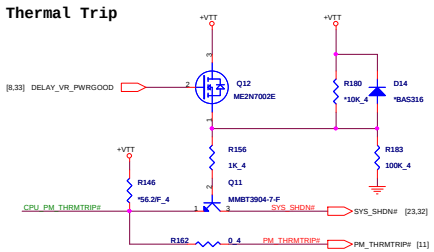


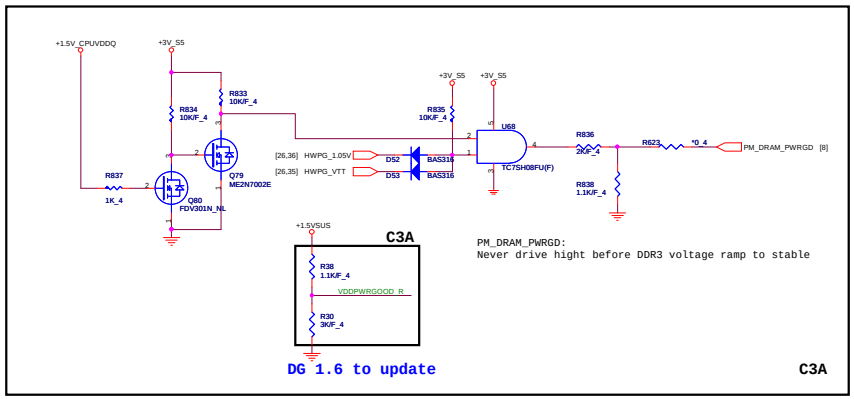
If R65 no stuff must change R61 to 50 ohm

CPU FAN CTRL



Thermal Trip





Quanta Computer Inc.
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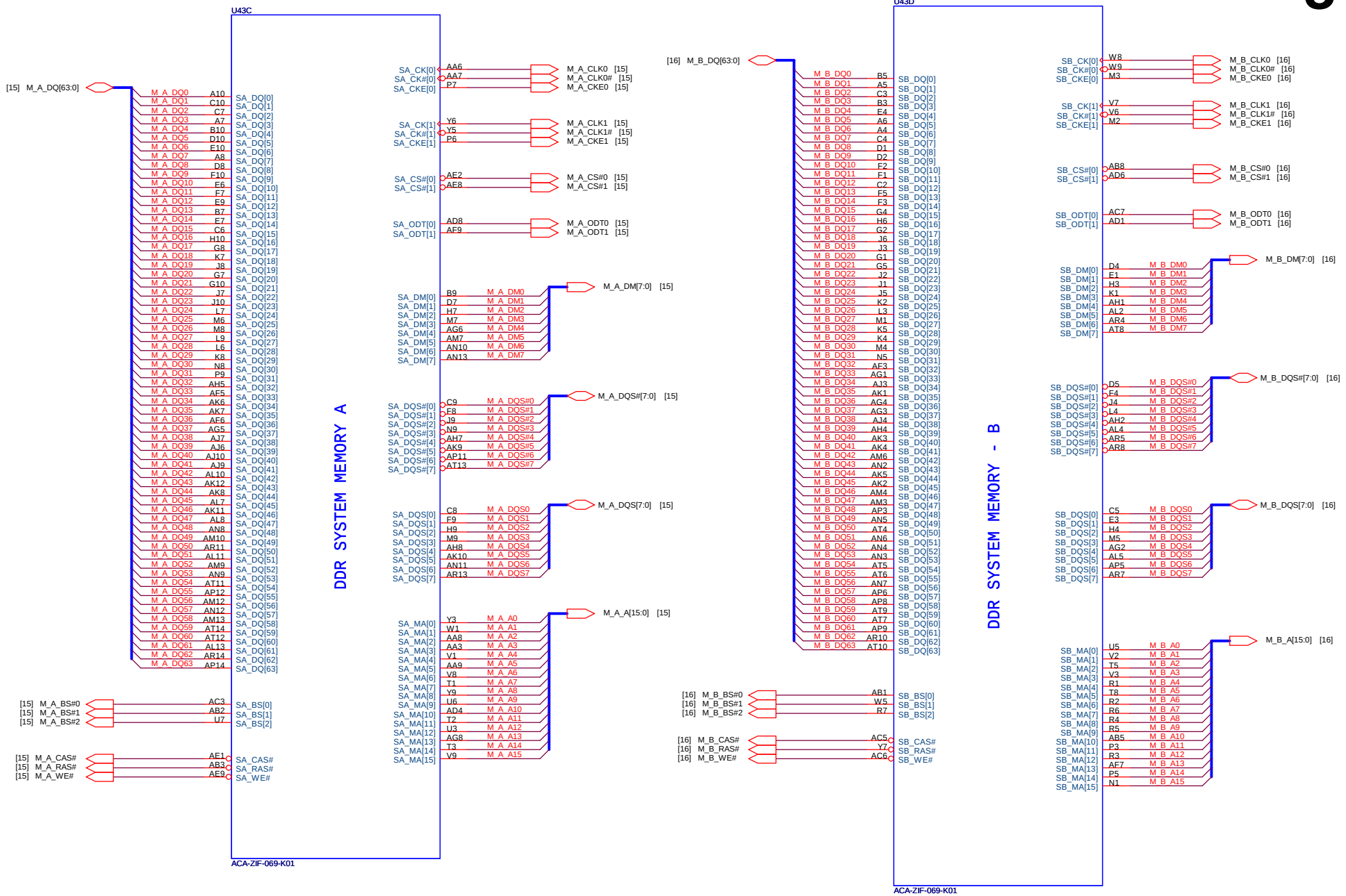
[CPU]

AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)

5



Quanta Computer Inc.

PROJECT : TZ1C

Size	Document Number	Rev
	PROCESSOR 2/4(DDR3)	B2A

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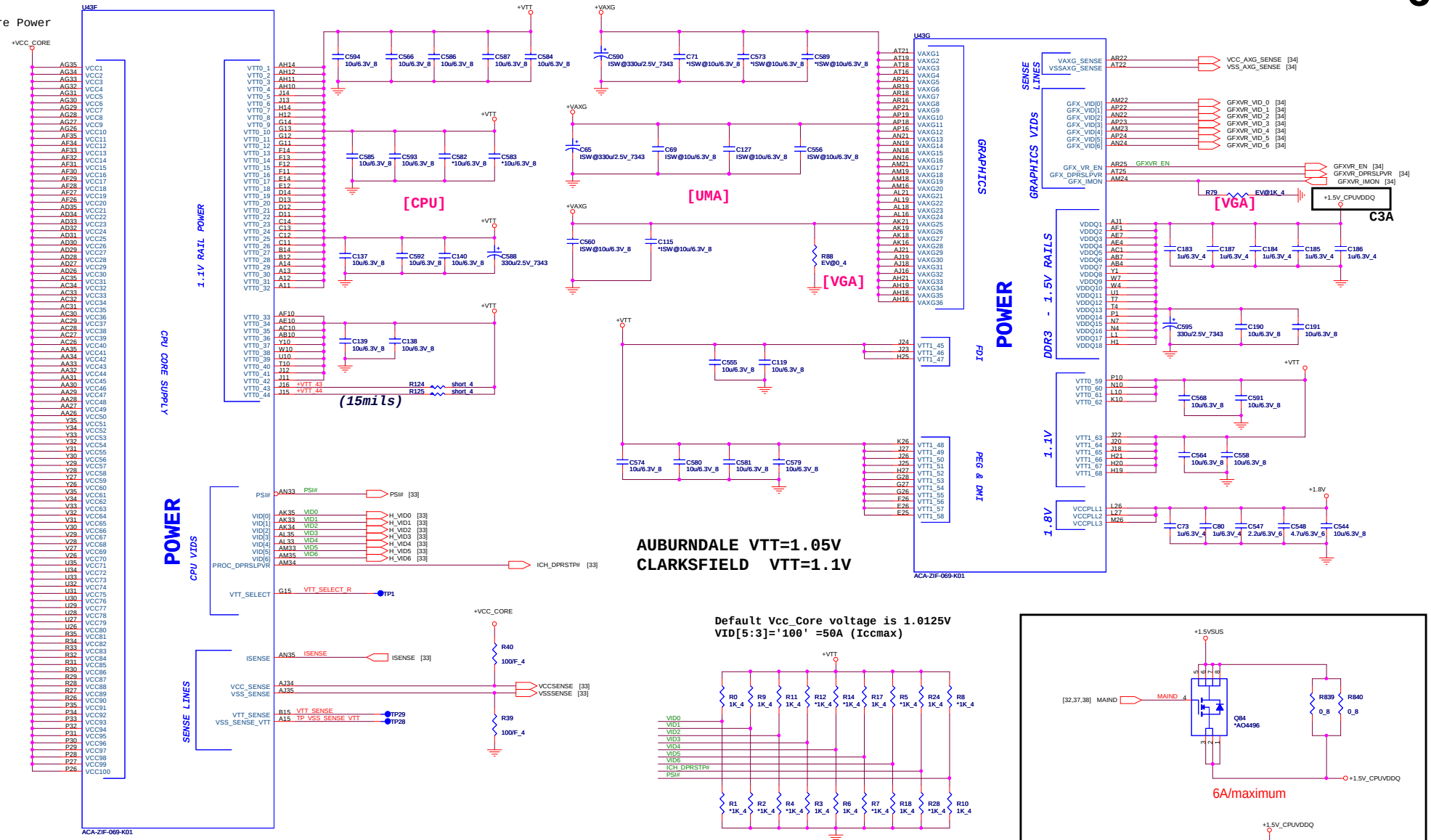
[CPU]

AUBURNDALE/CLARKSFIELD PROCESSOR (POWER)

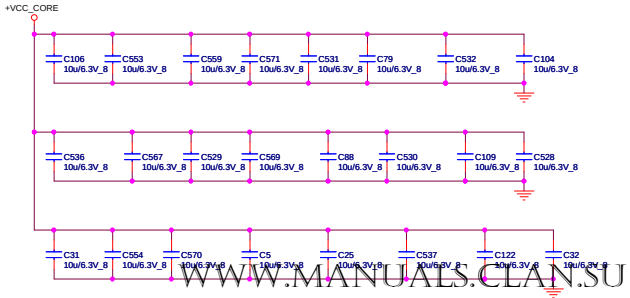
AUBURNDALE/CLARKSFIELD PROCESSOR (GRAPHICS POWER)

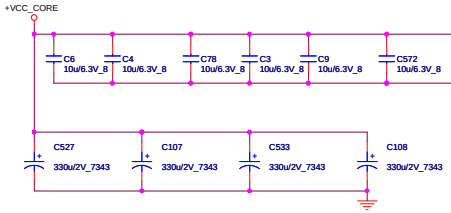
6

CPU Core Power



Default Vcc_Core voltage is 1.0125V
VID[5:3]='100' =50A (Iccmax)





Quanta Computer Inc.
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Size	Document Number	Rev
	PROCESSOR 3/4(POWER)	B2A

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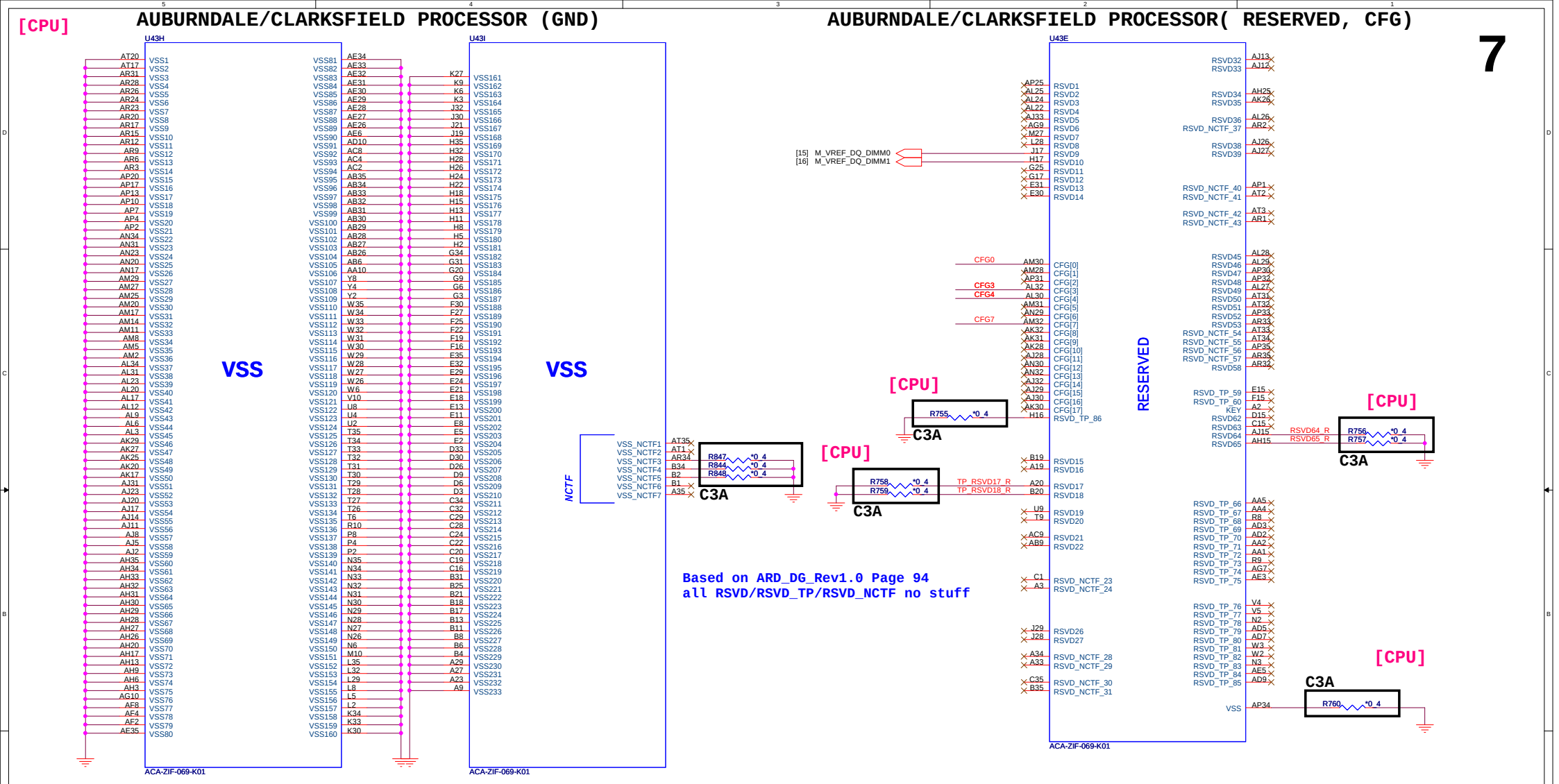
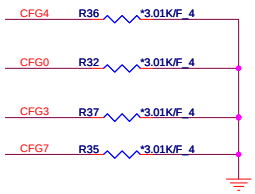


Processor Strapping



	1	0	DEFAULT
CFG4 (Embended Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port	1
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled	1
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed	1

Quanta Computer Inc.
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	PROCESSOR 4/4(GND)	B2A

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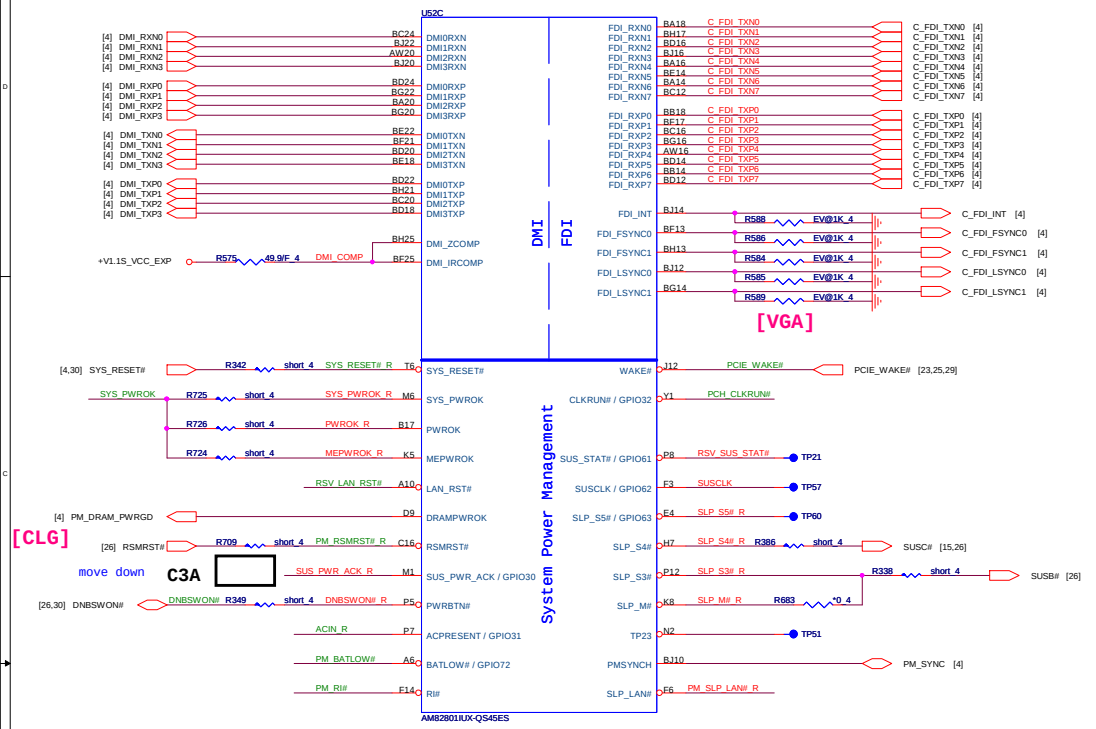
[CLG]

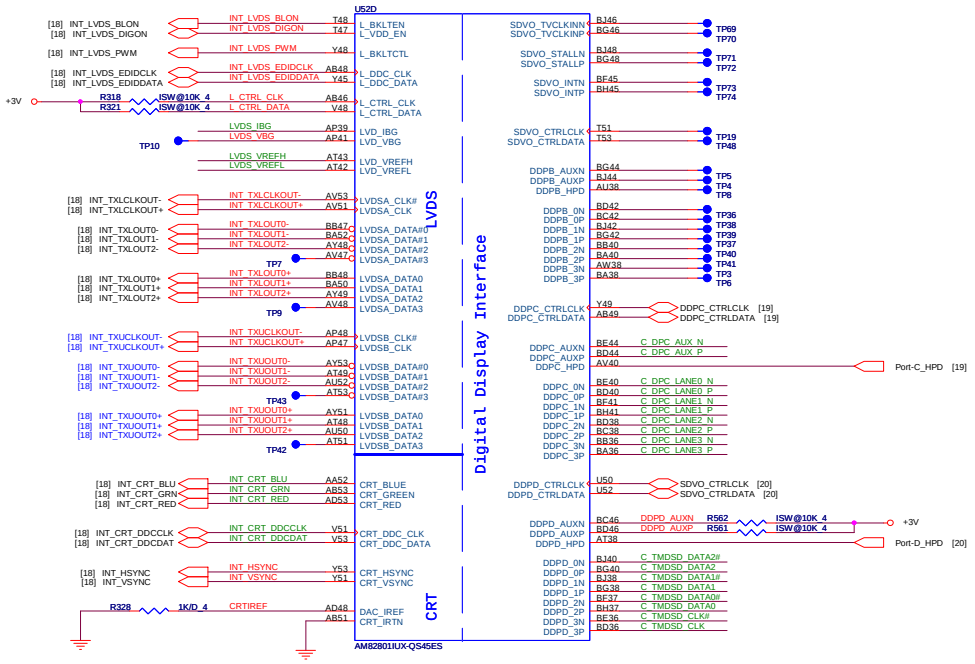
IBEX PEAK-M (DMI,FDI,GPIO)

Both FDI and DMI Supports Lane Reversal but only at PCH side enable via PCH soft strap

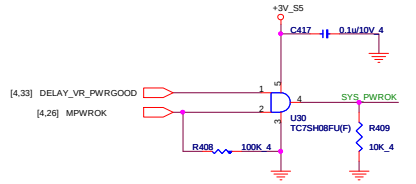
IBEX PEAK-M (LVDS,DDI)

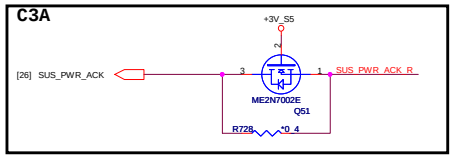
8

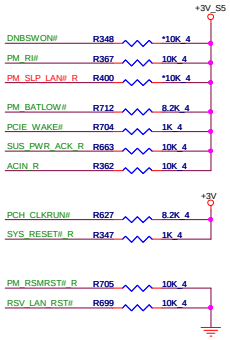


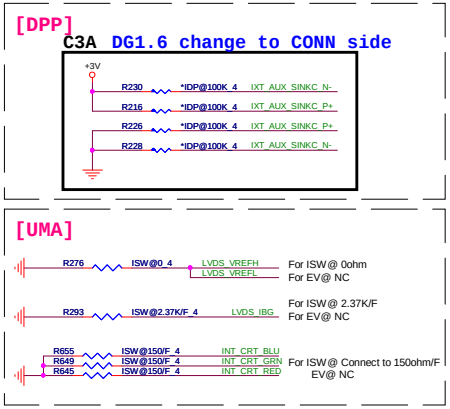


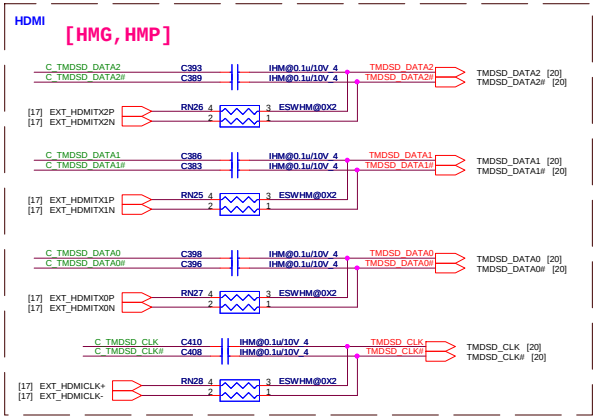
Port	Strap	How to enable Port?	How to disable Port?
LVDS	L_DDC_DATA	PU to 3.3V with 2.2k+/- 5%	NC
Port B	SDVO_CTRLDATA	PU to 3.3V with 2.2k+/- 5%	NC
Port C	DDPC_CTRLDATA	PU to 3.3V with 2.2k+/- 5%	NC
Port D	DDPD_CTRLDATA	PU to 3.3V with 2.2k+/- 5%	NC
eDP	CFG[4]	PD to GND directly	NC

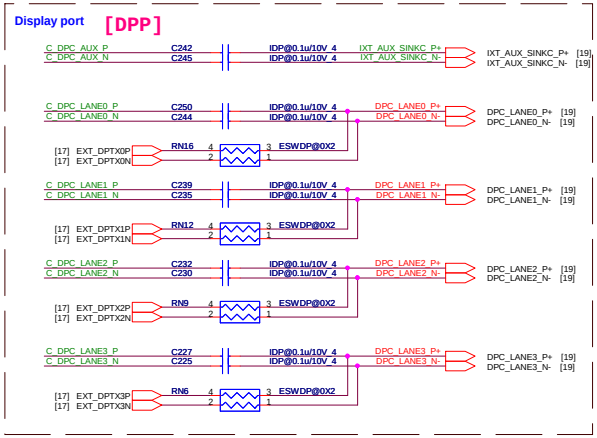












DisplayPort
Switchable: SW+DP and ESWDP
VGA:EDP
UMA:IDP

HDMI
Switchable: SW+HM and ESWHM
VGA:EHM
UMA:IHM

Quanta Computer Inc.
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	PCH 1/6(DMI&VIDEO&FDI&PM)	B2A
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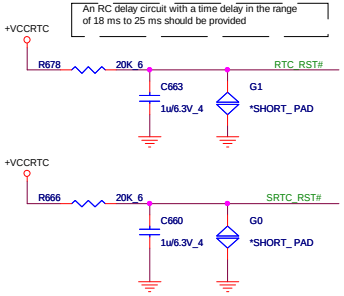
IBEX PEAK-M (HDA,JTAG,SATA)
[HM55 can not use SATA port2,3]

9

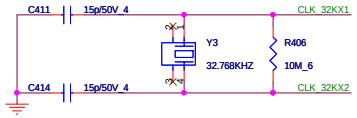
[CLG]

RESET JUMP

An RC delay circuit with a time delay in the range of 18 ms to 25 ms should be provided

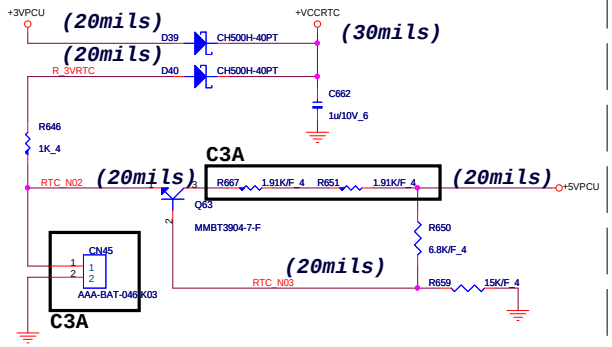


RTC CRYSTAL

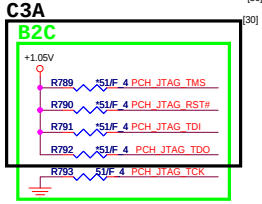


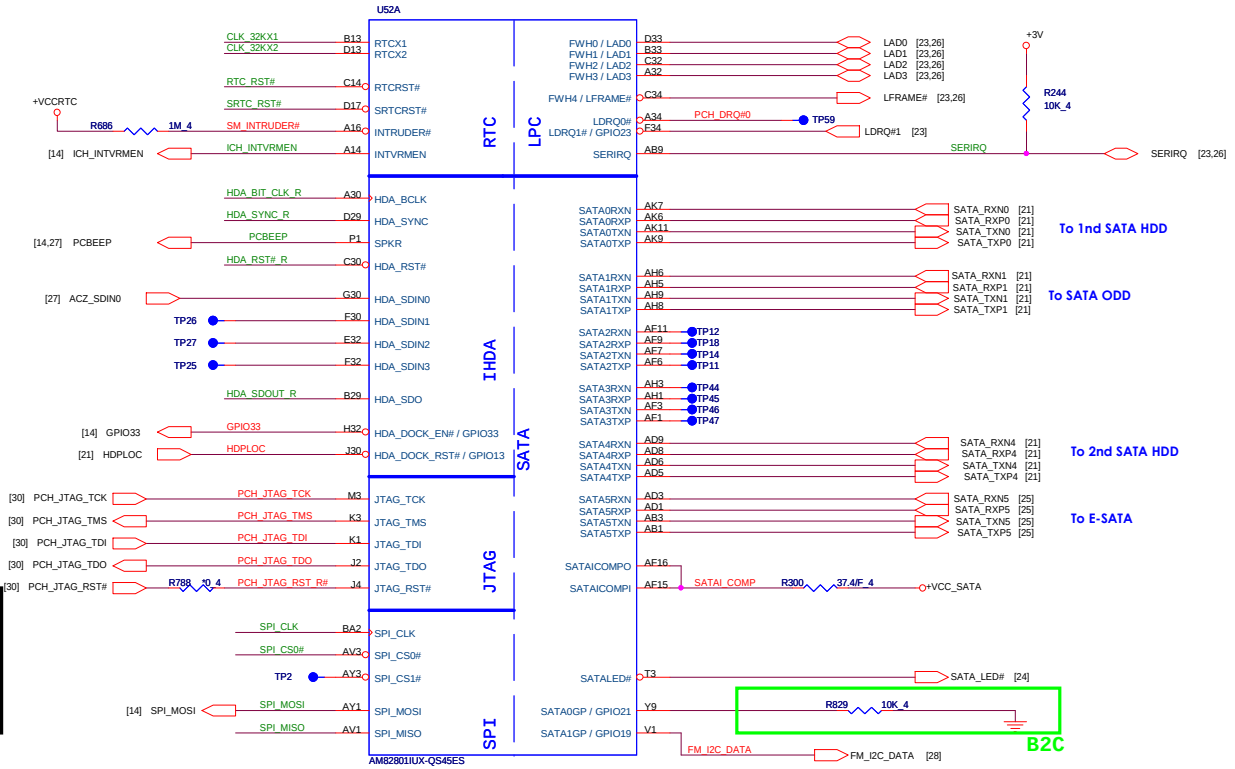
[RTC]

RTC BATTERY

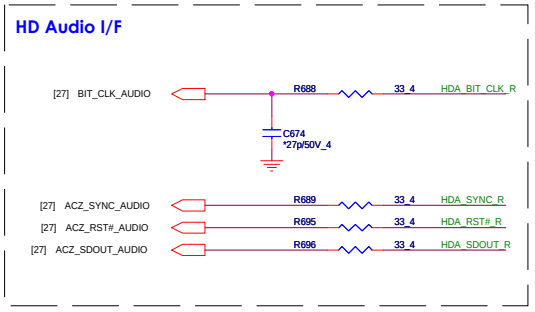


C3A B2C





HD Audio I/F



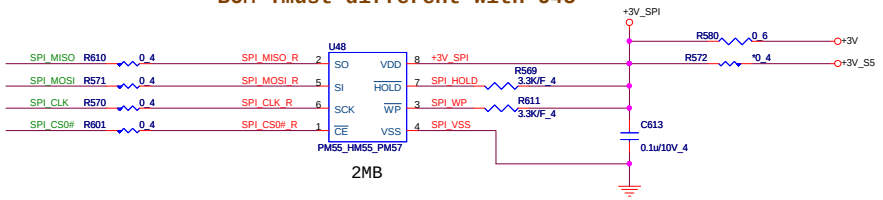
Note:Based on WW11 MoW.
only R793 default stuff others no stuff

[BIOS&ME]

Default PM55 for clarksfield

Winbond: 8MB/SOIC8-->[W25Q64BVSSIG]
4MB/SOIC8-->[W25X40AVSSIG]
2MB/SOIC8-->[W25Q16AVSSIG]

BOM :must different with U45



2MB

PCH	2MB	4MB	8MB
PM55	●		
HM55		●	
HM57/PM57		●	●
QM57/QS57			●

Quanta Computer Inc.
PROJECT : TZ1C

Size	Document Number	Rev
	PCH 2/6 (SATA,LPC,SPI,HD)	B2A
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[CLG]

IBEX PEAK-M (PCI,USB,NVRAM)
[HM55 can not use USB port6,7]

IBEX PEAK-M (PCI-E,SMBUS,CLK)

10

If no implement BW let as NC
include NV_RCOMP

D3A

Note:Port6 is for Intel LAN use
so B stage change to Port7

EHCI#1
EHCI#2

C3A

R715/R850/R851 stuff
OC4/OC6 tire together
OC3 for USB_BUS_SW3

R850/R852/R853 stuff
OC3/OC4 tire together
OC2 for USB_BUS_SW3

USB0C5# use for USB Board
USB0C6# use for E-SATA & USB

TO VGA RST

TO other device

Note:PCIECLKRQ[2:1]# on PCH are core well power

C3A:Change by vender report

B2C

B2C

Quanta Computer Inc.
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Size | Document Number: PCH 3/6 (PCI,USB,CLK,SMB) | Rev: B2A
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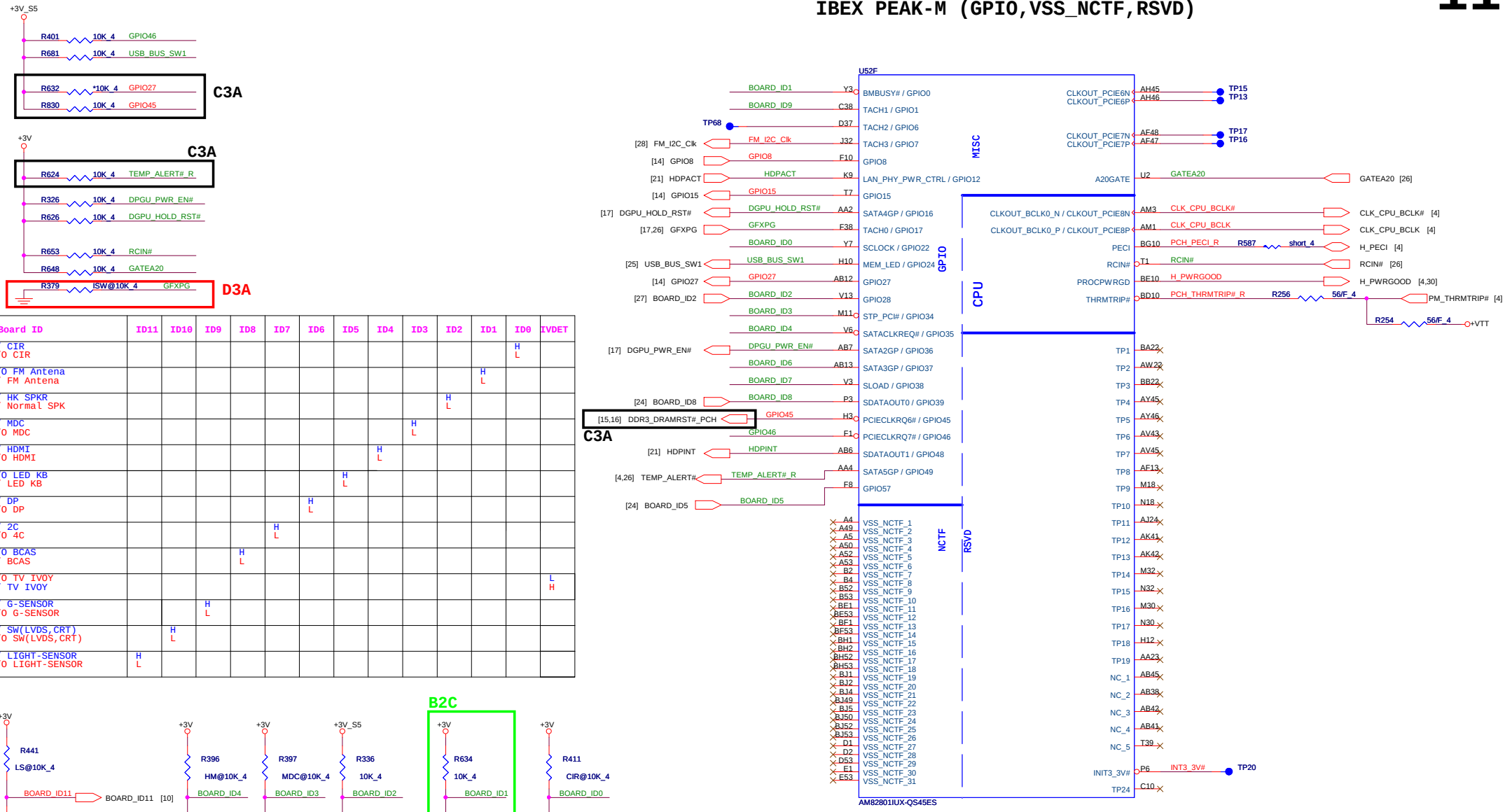
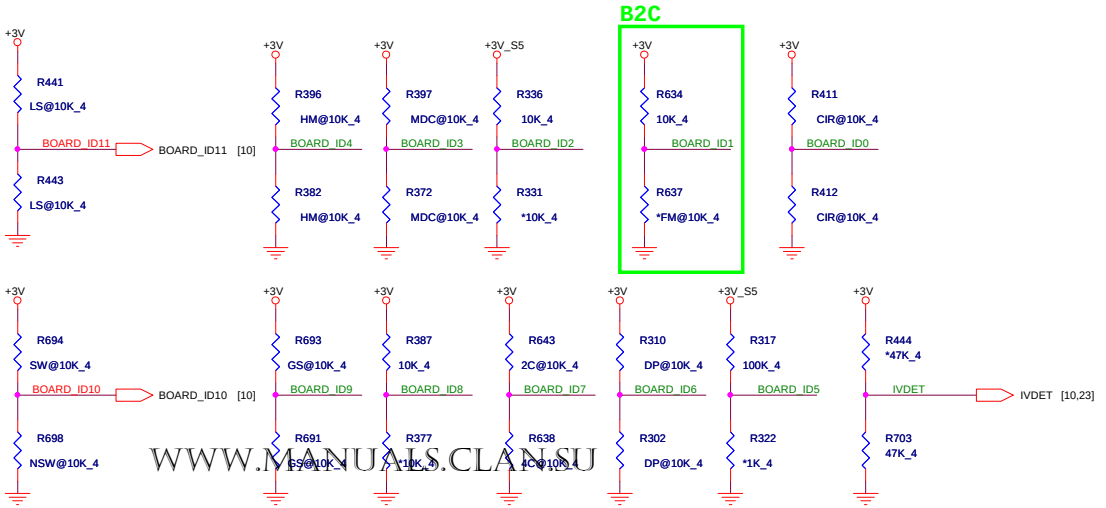
IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



Board ID	ID11	ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	IVDET
W/ CIR W/O CIR												H L	
W/O FM Antena W/ FM Antena											H L		
W/ HK SPKR W/ Normal SPK										H L			
W/ MDC W/O MDC									H L				
W/ HDMI W/O HDMI								H L					
W/O LED KB W/ LED KB							H L						
W/ DP W/O DP						H L							
W/ 2C W/O 4C					H L								
W/O BCAS W/ BCAS				H L									
W/O TV IVOY W/ TV IVOY													L H
W/ G-SENSOR W/O G-SENSOR			H L										
W/ SW(LVDS,CRT) W/O SW(LVDS,CRT)		H L											
W/ LIGHT-SENSOR W/O LIGHT-SENSOR	H L												



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Size	Document Number	Rev
	PCH 4/6 (GPIO)	B2A
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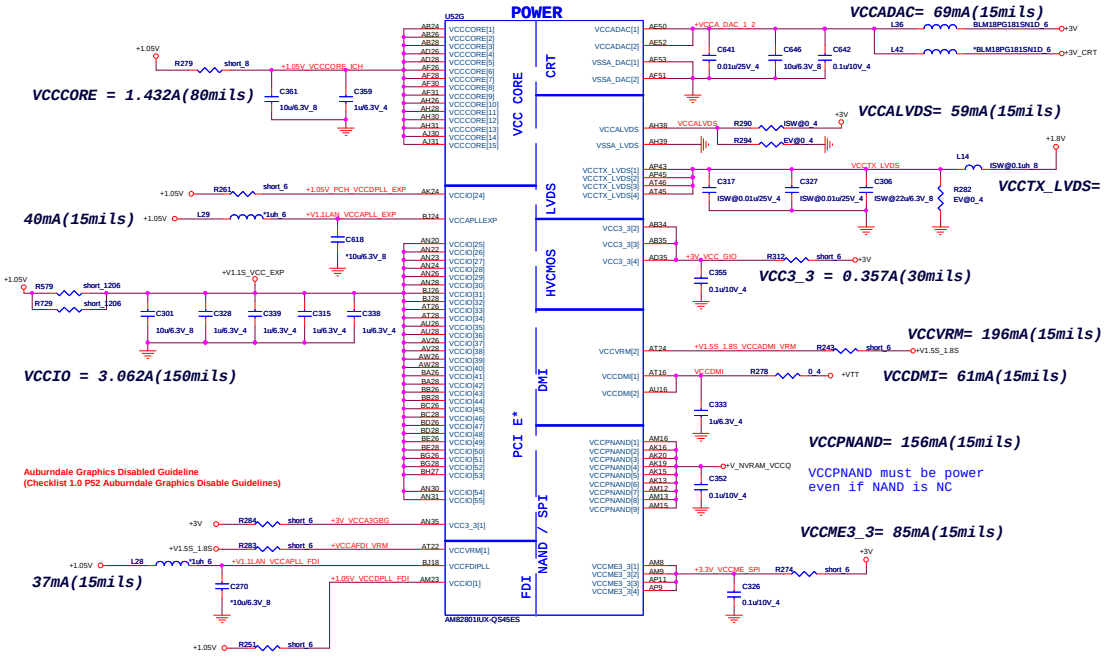
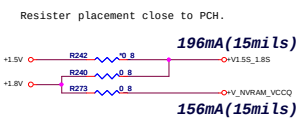
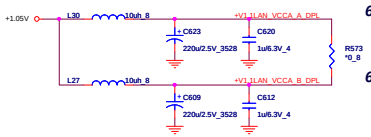
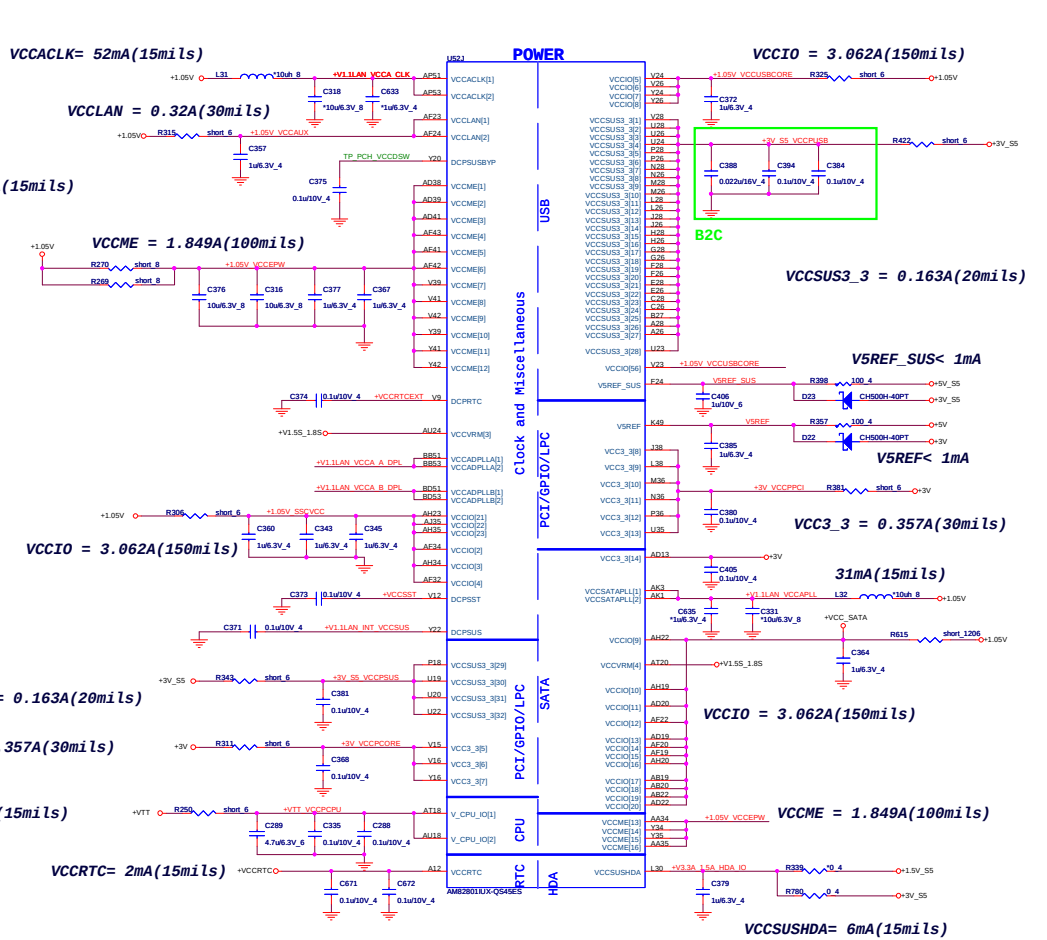




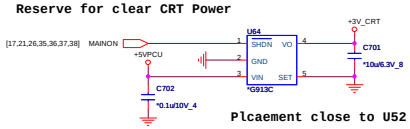
VCCVRM can be 1.5V or 1.8V for internal PLL and VRMs
VccpNAND is 1.8V for dual Channel NAND interface



VRM enable by strap pin GPIO27
which supply clean 1.05V for
[VCCACLK,VCCAPLLEXP,VCCFDIPLL,VCCSATAPLL]



Reserve for clear CRT Power



Quanta Computer Inc.		
PROJECT : TZ1C		
Size	Document Number: PCH 5/6 (POWER)	Rev: B2A
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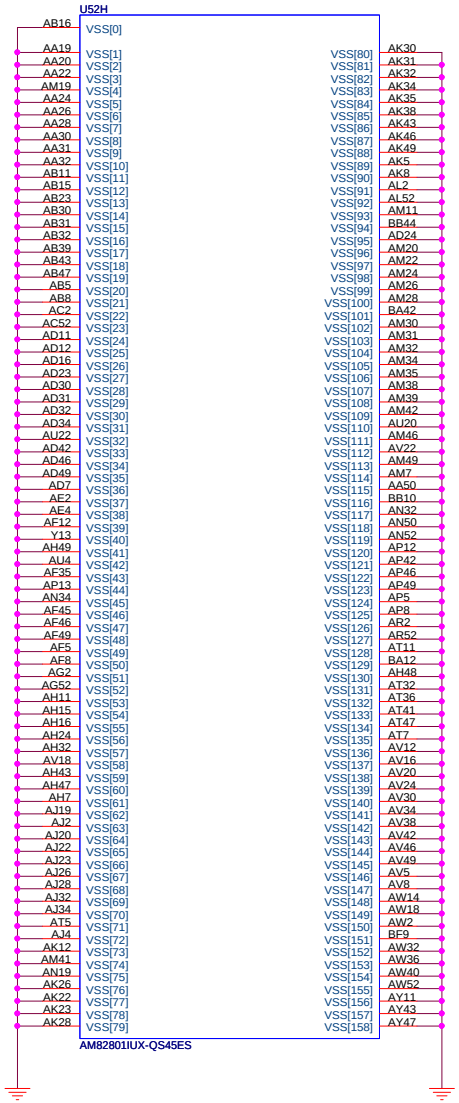
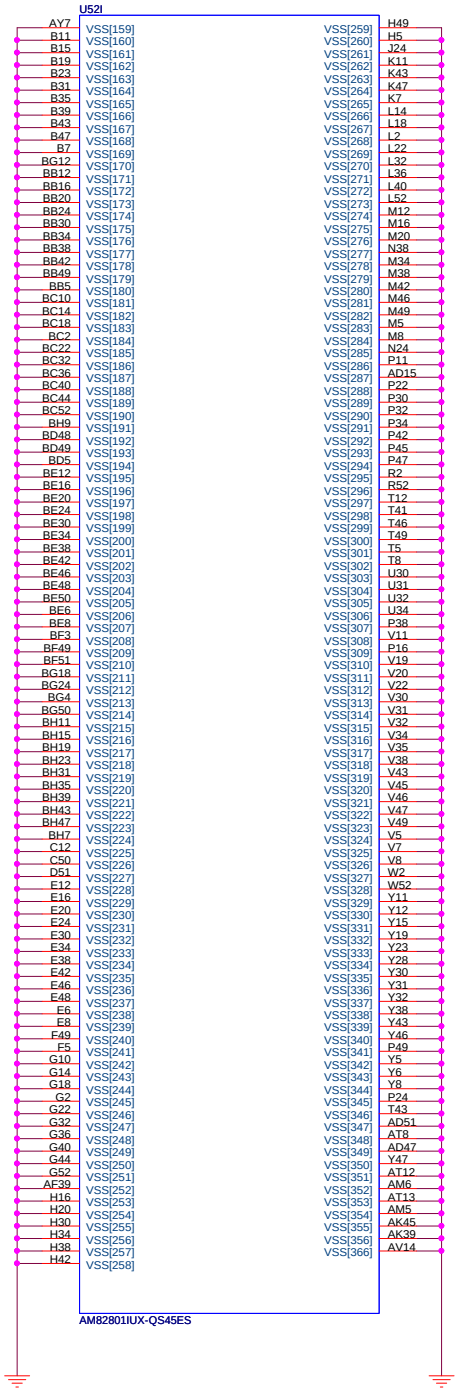
IBEX PEAK-M (GND)





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	PCH 6/6 (GND)	B2A
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PCH Strap Pin Configuration Table [CLG]

(See PCH EDS Page.80)

Pin Name	Strap description	Configuration	Setting	when sampled
SPKR	Reboot option at power-up	0 = Default Mode (Internal weak Pull-down) 1 = No Reboot Mode with TCO Disabled	[9,27] PCBEEP — R388 *10K_4 — +3V	Rising edge of PWROK
INIT3_3V#	Reserved	Weak internal pull-down. Do not pull high.		Rising edge of PWROK
GNT3#/ GPIO55	Top-Block Swap Override	0 = Top Block Swap Mode 1 = Default Mode (Internal pull-up)	[10] PCI_GNT3# — R665 *1K_4 — GND	Rising edge of PWROK
INTVRMEN	Integrated 1.05V VRM Enable / Disable	1 = Integrated VRM is enabled 0 = Integrated VRM is disabled	[9] ICH_INTVRMEN — R654 332K/F_4 — +VCCRTC	Always
GNT0#, GNT1#	Boot BIOS Strap	(0,0) = LPC (0,1) = Reserved NAND (1,0) = PCI (1,1) = SPI	[10] PCI_GNT0# — 1K_4 R368 [10] PCI_GNT1# — 1K_4 R358 — GND	Rising edge of PWROK
SPI_MOSI	TPM Functionality Disable	1 = Enabled 0 = Disable	[9] SPI_MOSI — R594 *TPM@1K_4 — +3V	Rising edge of MEPWROK
NV_ALE	IntelR Anti-Theft Technology HDD Data Protection (Intel AT-d) Enable	1 = Enabled 0 = Disabled (Default)	[10] NV_ALE — R583 *10K_4 — +V_NVRAM_VCCQ	Rising edge of PWROK
NV_CLE	DMI Termination Voltage	DMI termination voltage. Weak internal pull-up. Do not pull low.		Rising edge of PWROK
HDA_DOCK_EN #/GPIO33	Flash Descriptor Security Override	0 = Flash Descriptor Security will be overridden 1 = Security measure defined in the Flash Descriptor will be enabled.	[9] GPIO33 — R410 100K_4 — GND	Rising edge of PWROK
HDA_SDO	Reserved	This signal has a weak internal pull down. NOTE: This signal should not be pulled high		Rising edge of RSMRST#
GPIO8	Reserved	This signal has a weak internal pull up. NOTE: This signal should not be pulled low	[11] GPIO8 — R713 10K_4 — +3V_S5	Rising edge of RSMRST#
HDA_SYNC	Reserved	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.		Rising edge of RSMRST#
GPIO15	Reserved	0 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality 1 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality	[11] GPIO15 — R383 1K_4 — +3V_S5	Rising edge of RSMRST#
GPIO27	On-Die PLL Voltage Regulator	0 = Disables the VccVRM. Need to use on-board filter circuits for analog rails. 1 = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. This signal has a weak internal pull-up.	[11] GPIO27 — R330 *10K_4 — GND	Rising edge of RSMRST#
GNT2#/ GPIO53	ESI Strap (Server Only)	Tying this strap low configures DMI for ESI compatible operation. This signal has a weak internal pull-up.		Rising edge of PWROK

Boot BIOS Strap

PCI_GNT0#	PCI_GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

Quanta Computer Inc.

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	PCH STRAP	B2A

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[DDR]

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JDIM1A

PC2100 DDR3 SDRAM SO-DIMM (204P)

DDRRK-20401-TP5B

JDIM1B

PC2100 DDR3 SDRAM SO-DIMM (204P)

DDRRK-20401-TP5B

follow DG 1.5 update

Place these Caps near So-Dimm0.

M1: Fixed SO-DIMM VREF_DQ [Arrandale/ES/QS]

M3:Processor Generated SO-DIMM VREF_DQ [Clarksfield/QS]

not required for ARD only

C3A

B2C

M2: Programmable SO-DIMM VREFDQ (Used for >1066MT/s) [Clarksfield/ES]

[VGA]

ISL90727 I2C Address is 5CH

M2 no stuff

C3A

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Size	Document Number	Rev
	DDR3 DIMM-0	B2A
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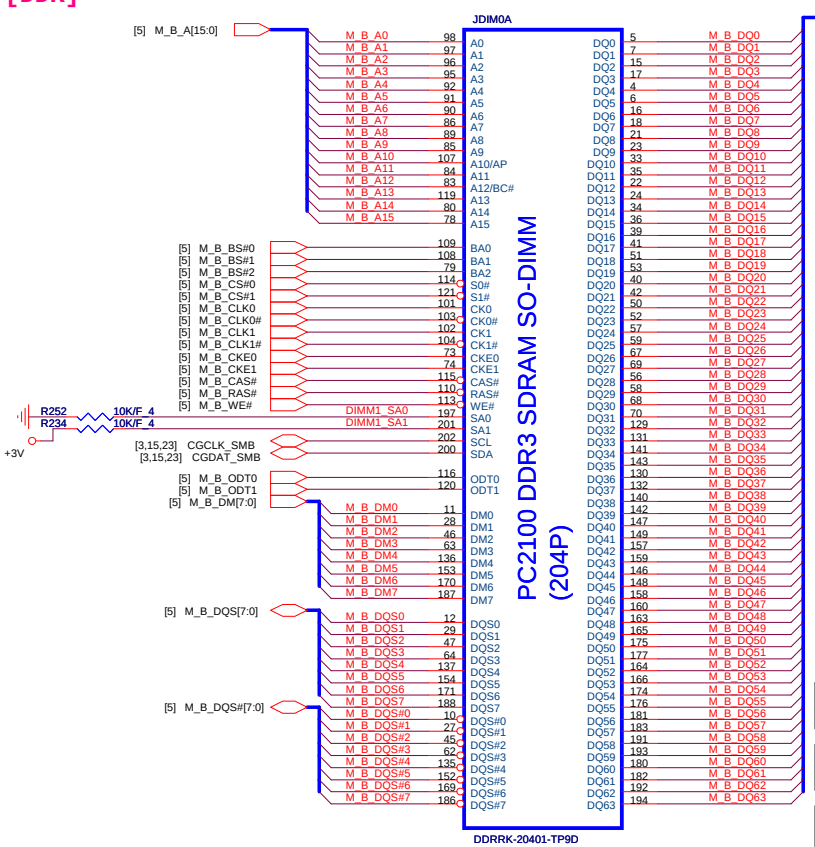
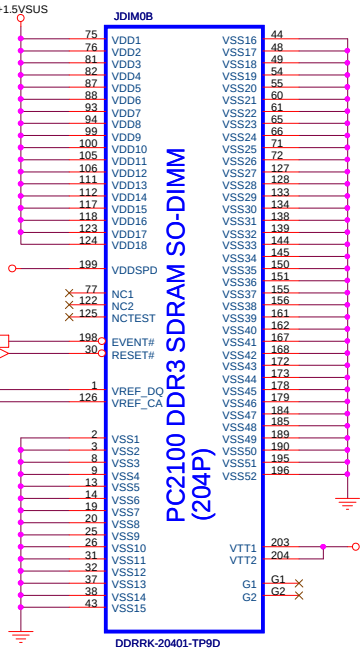
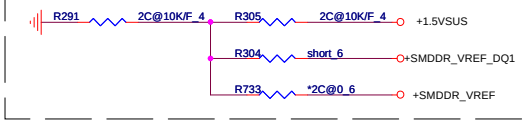
[DDR]



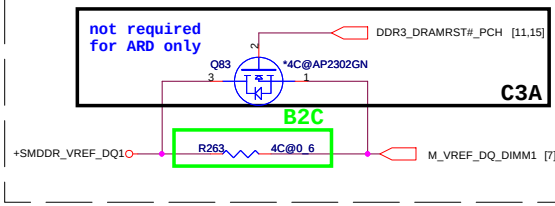


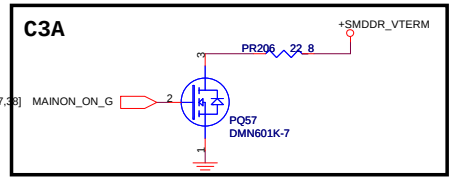
16

M1: Fixed SO-DIMM VREF_DQ [Arrandale/ES/QS]

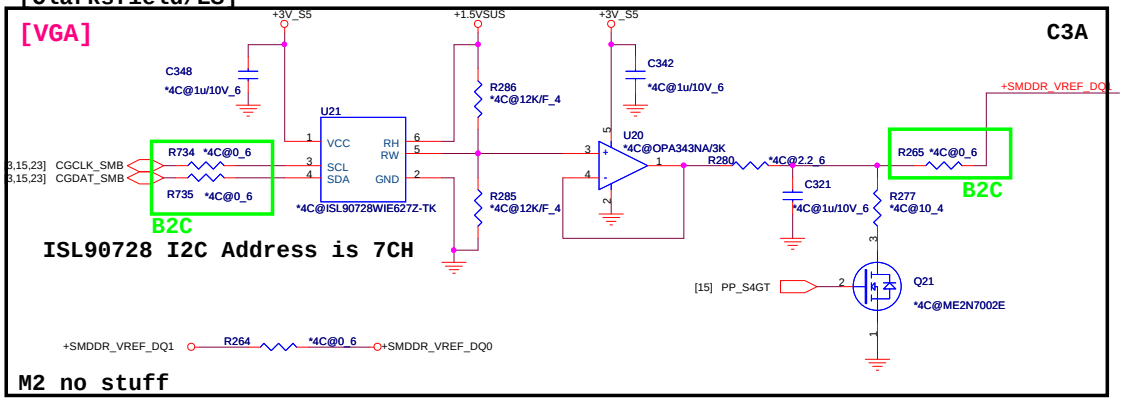


M3:Processor Generated SO-DIMM VREF_DQ [Clarksfield/QS]

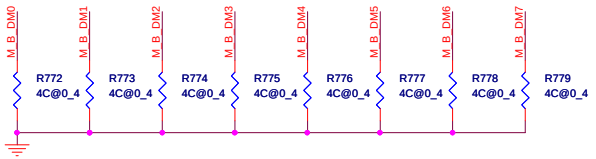




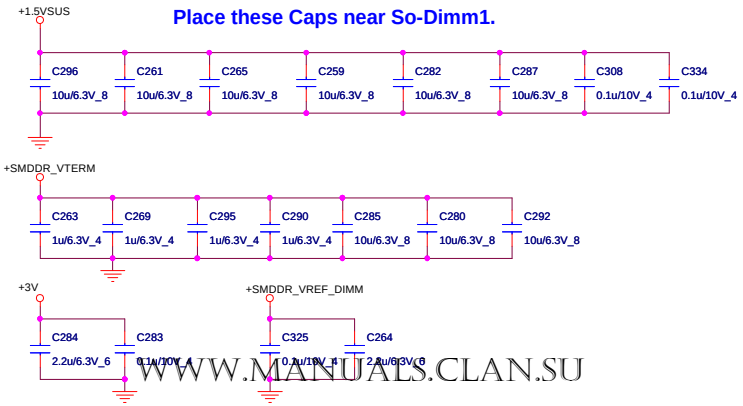
M2: Programmable SO-DIMM VREFDQ (Used for >1066MT/s) [Clarksfield/ES]

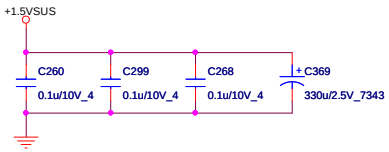


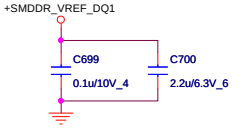
follow DG 1.5 update



Place these Caps near So-Dimm1.







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Size	Document Number	Rev
	DDR3 DIMM-1	B2A
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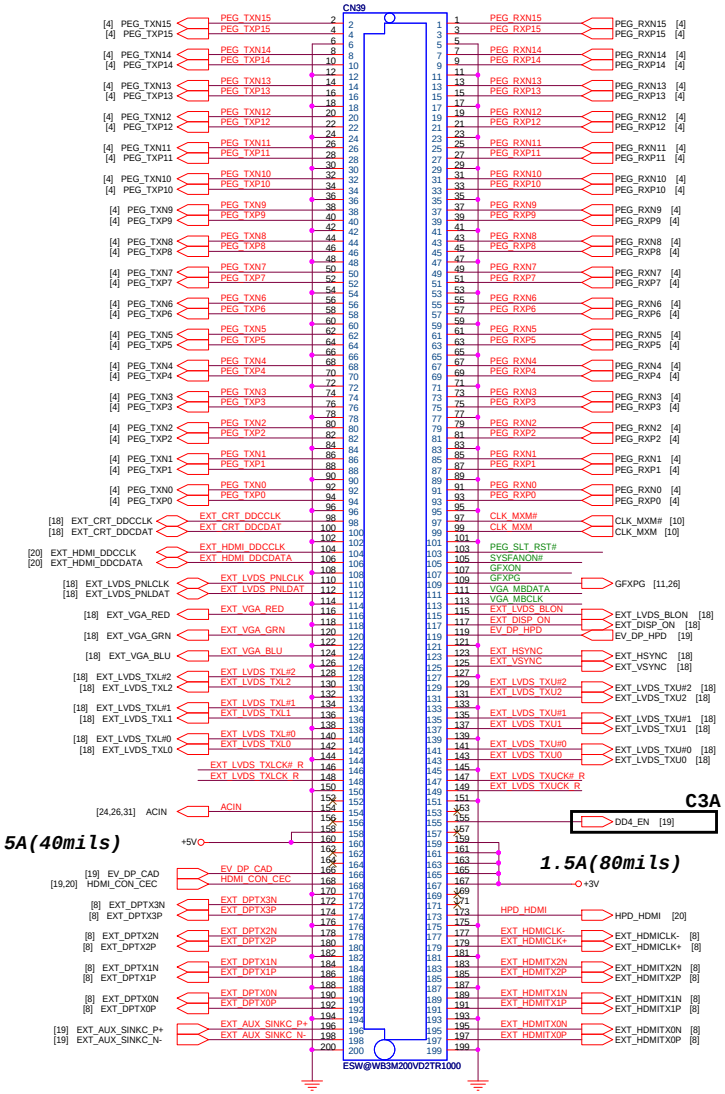
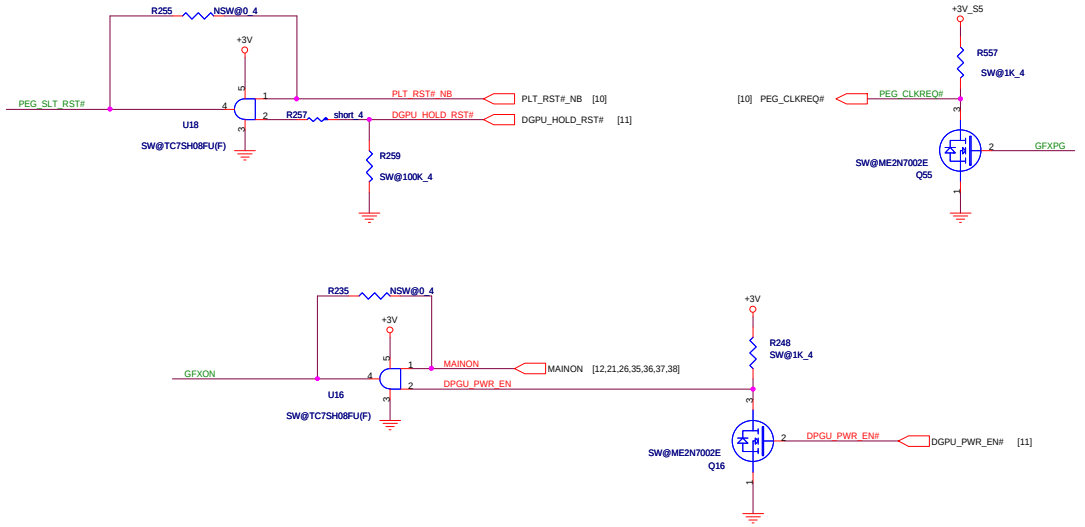
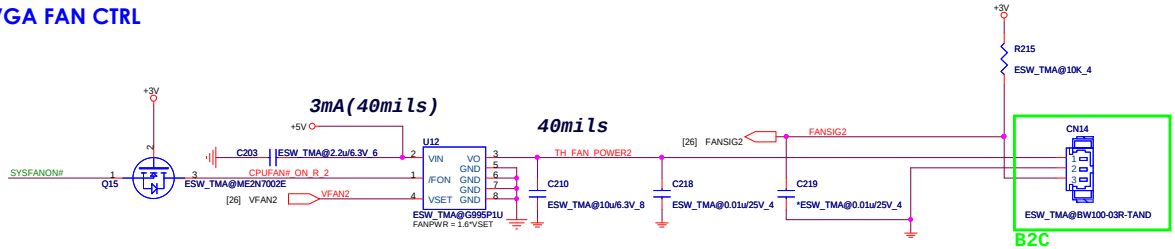
VGA BOARD CONNECOTR
[VGA]

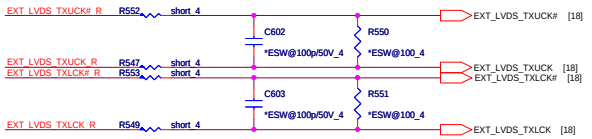


VGA switchable control
[GSW]

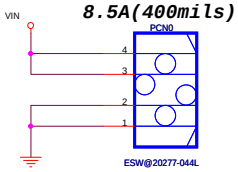


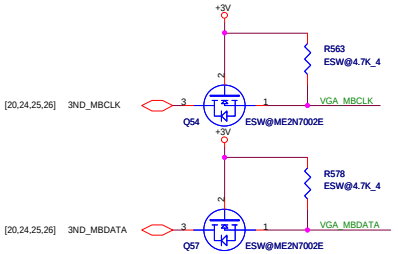
VGA FAN CTRL

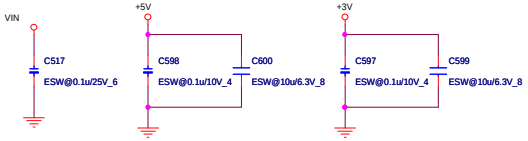




VGA Power conn







Quanta Computer Inc.
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Size	Document Number	Rev
	VGA CONNECTOR	B2A
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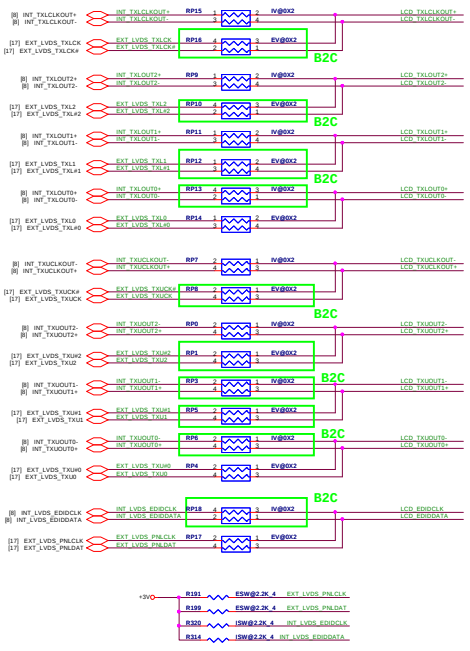
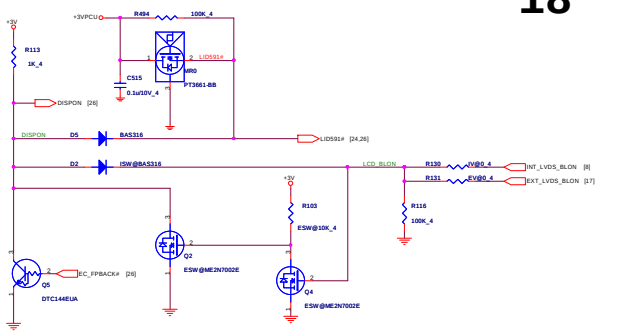
LVDS Signals [GSW]

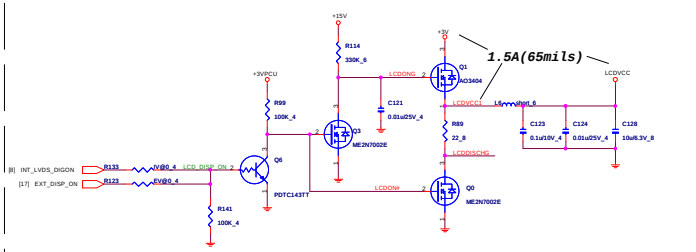
LVDS Signals [LDS]



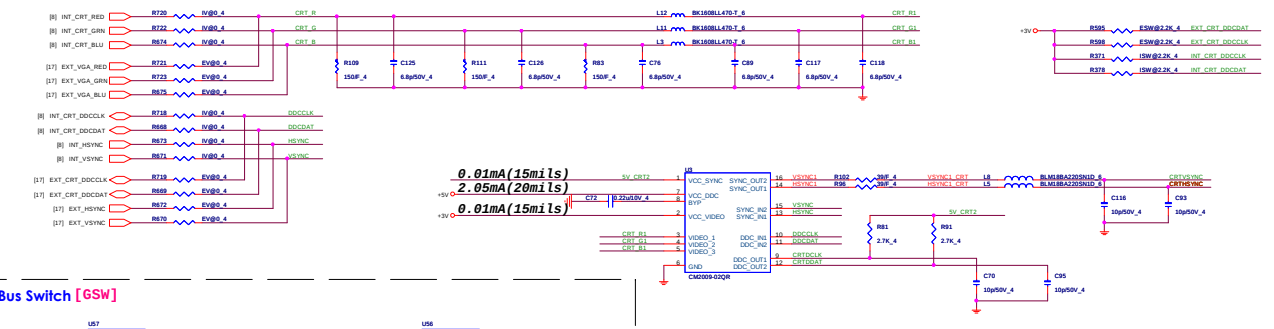
HALL SENSOR&BACK LIGHT SWITCH [HSR]



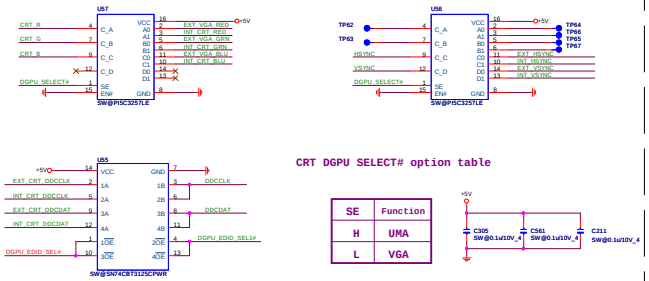
LCD POWER SWITCH [LDS]



CRT [CRT]



CRT Bus Switch [GSW]



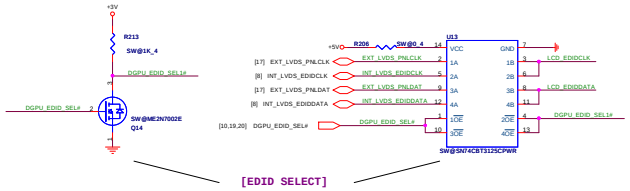
CRT DGPU SELECT# option table

SE	Function
H	UMA
L	VGA

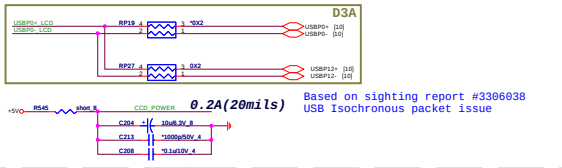
LVDS DGPU SELECT# option table

SEL[1:2]	Function
H	UMA
L	VGA

[EDID SELECT]

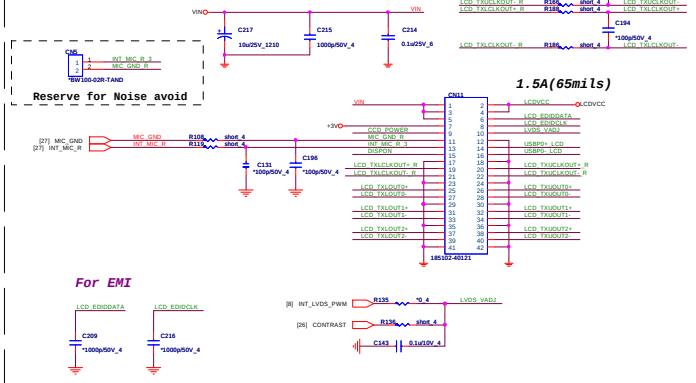


CCD [CCD]



Based on sighting report #3306038
USB Isochronous packet issue

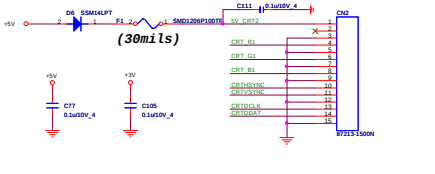
LCD Panel Module [LDS]

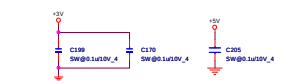


For EMI

[HSR]

[LDS]





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	LCD/LED Panel/CCD	82A
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DP redriver IC

[DPP]

DP redriver

U15 — DP@PI2EQXDP101ZFE

Note:DDPC_CTRLDATA=1 Port C detect
DDPC_CTRLDATA=0 Port C not detect

C3A

If U15 change to new version
R516 must change to 180K

[GSW]

SE	Function
H	UMA
L	VGA

U65 — SW@PI5C3257LE

U67 — SW@PI5C3257LE

ESD Protect

U44 — *DP@CM1213A-04SO

U46 — *DP@CM1213A-04SO

U14 — *DP@CM1213A-04SO

Close CONN

D18 — *DP@VPORT 0603 220K-V05

U10 — DP@G546B2P1UF

D15 — *DP@CH500H-40PT

Based on DG. 1.6/ P.146
change PU/PD to Conn side

Quanta Computer Inc.
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Size	Document Number	Rev
	Display Port	B2A

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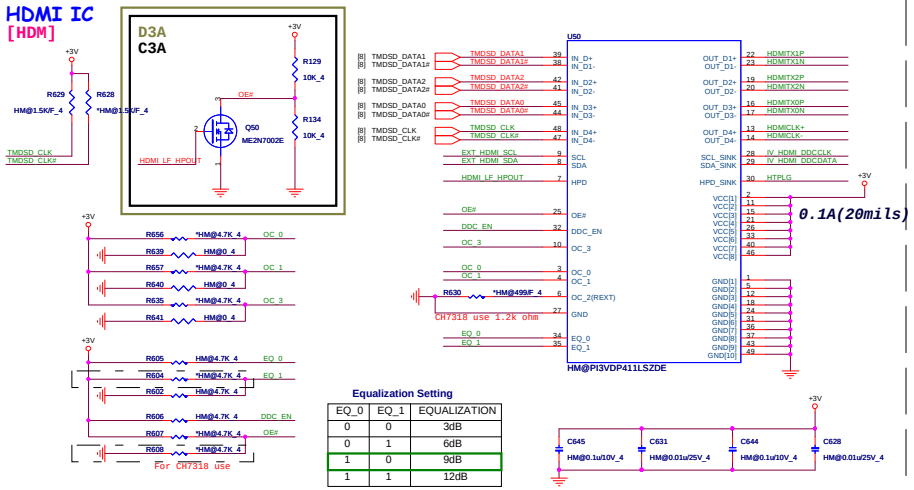
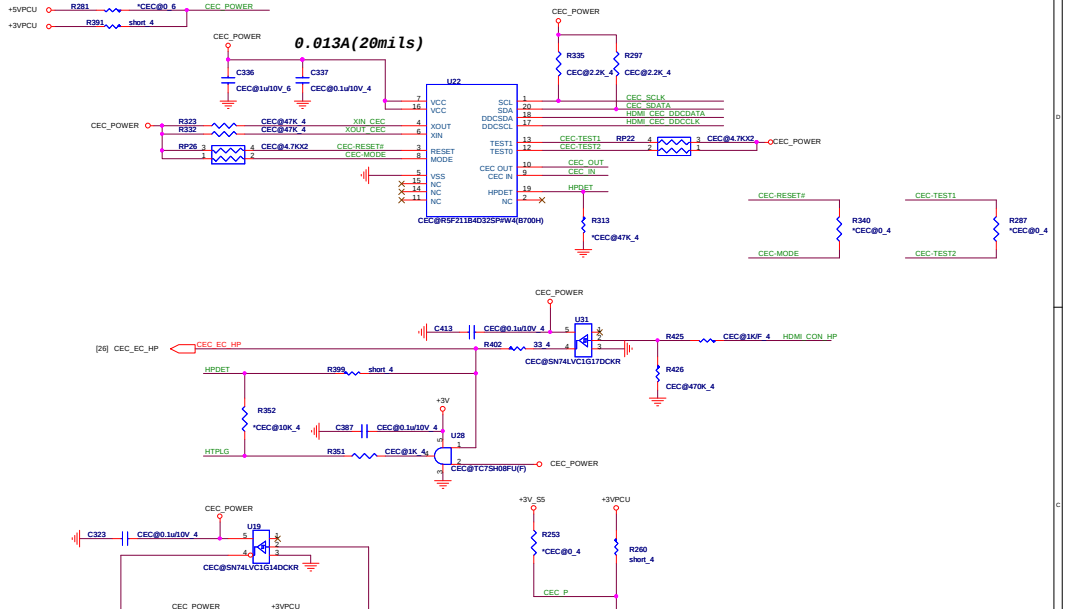
HDMI IC [HDM]



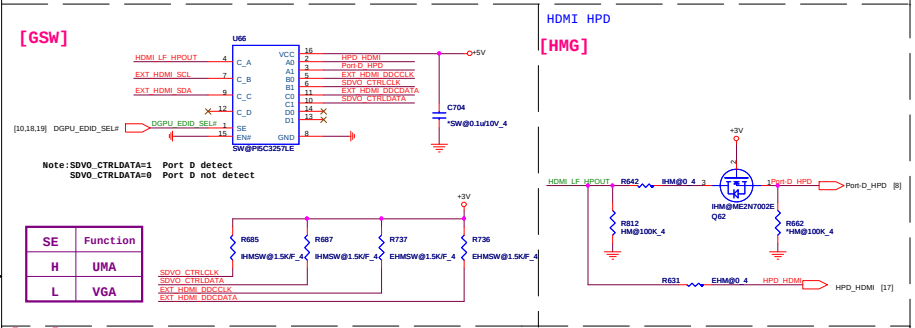
Equalization Setting

EQ_0	EQ_1	EQUALIZATION
0	0	3dB
0	1	6dB
1	0	9dB
1	1	12dB

HDMI CEC [HDM]



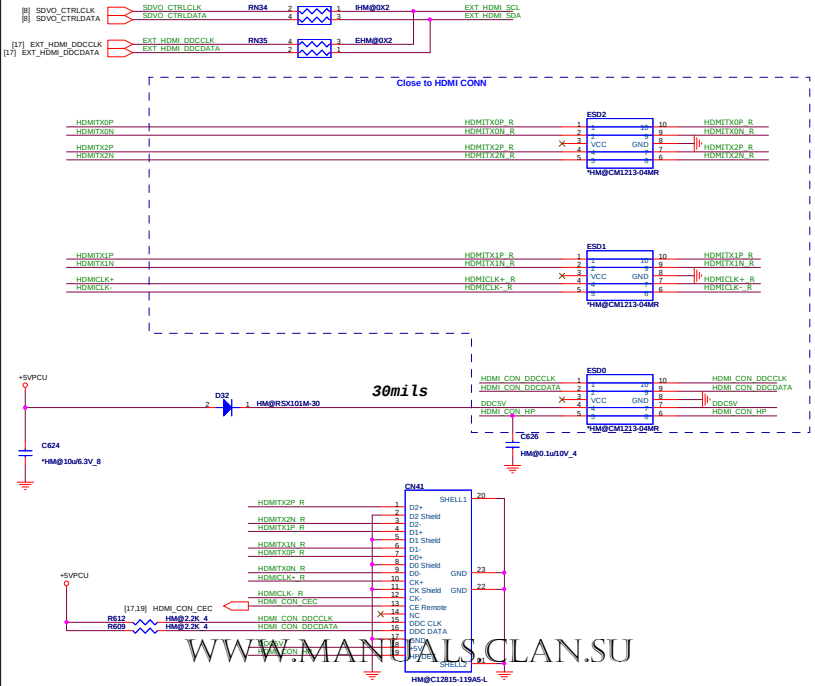
HDMI HPD [HMG]



Note:SDVO_CTRLDATA=1 Port D detect
SDVO_CTRLDATA=0 Port D not detect

SE	Function
H	UMA
L	VGA

[HDM]



Quanta Computer Inc.
PROJECT : TZ1C

Size	Document Number	Rev
	HDMI/CEC	82A

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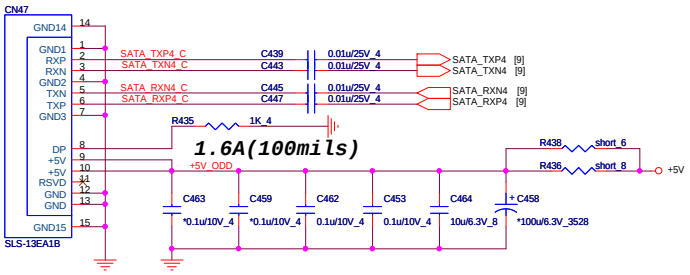
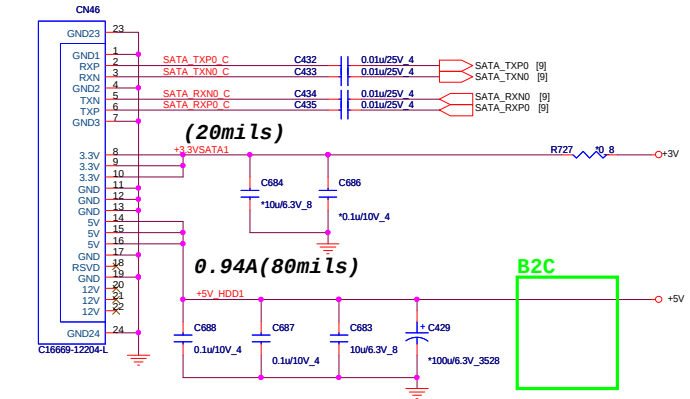
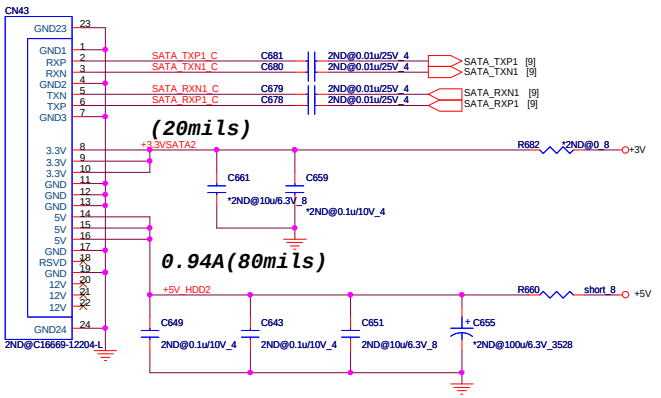
SATA ODD [ODD]



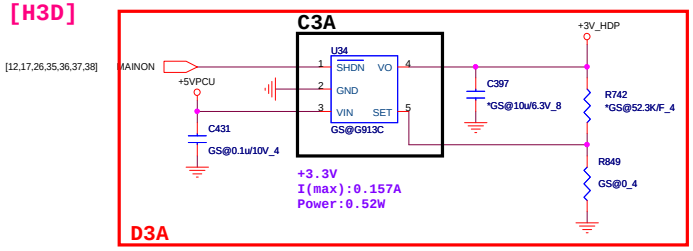
Main SATA HDD [HDD]

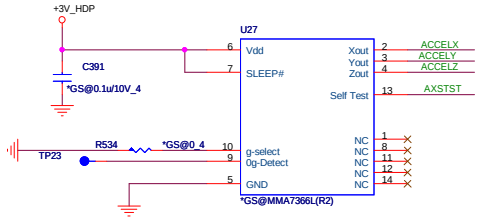


2nd SATA HDD [HDD]



G-sensor [H3D]





FS (Full Scale) selection

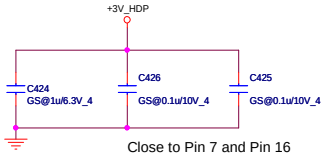
FS	0	1
	2g Full-Scale	6g Full-Scale

PD (Power Down) selection

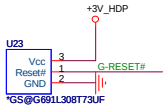
PD	0	1
	Normal Mode	Power-down mode

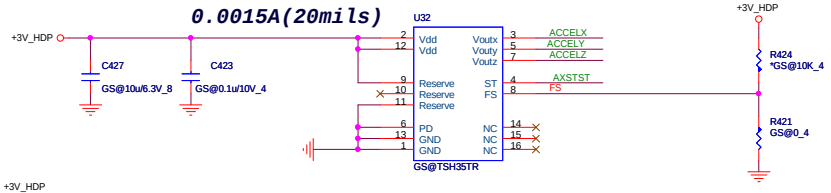
HDPPD selection

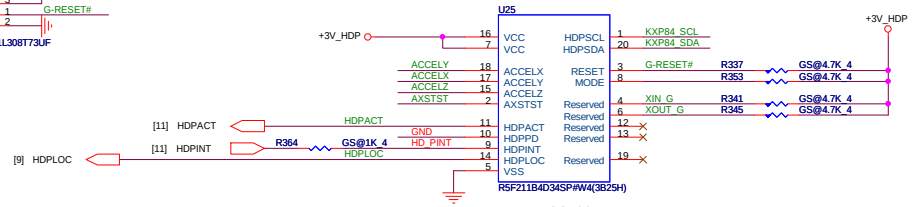
HDPPD	0	1
	Normal Mode	Power-down mode



Close to Pin 7 and Pin 16

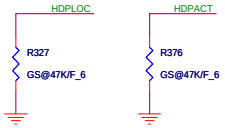




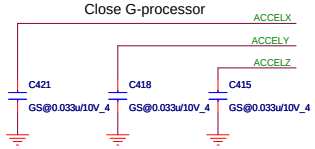


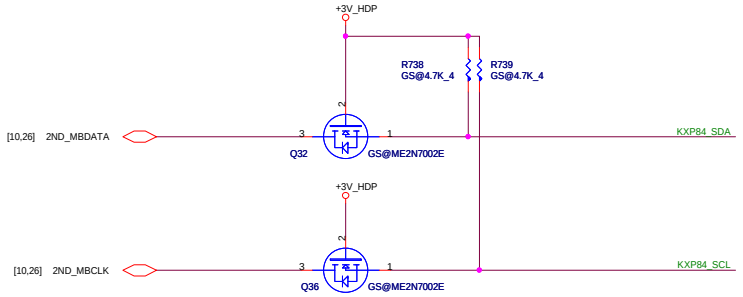
ADDRESS: 32H

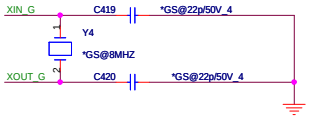
Close G-processor



Close G-processor







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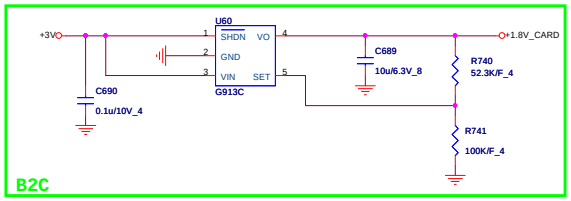
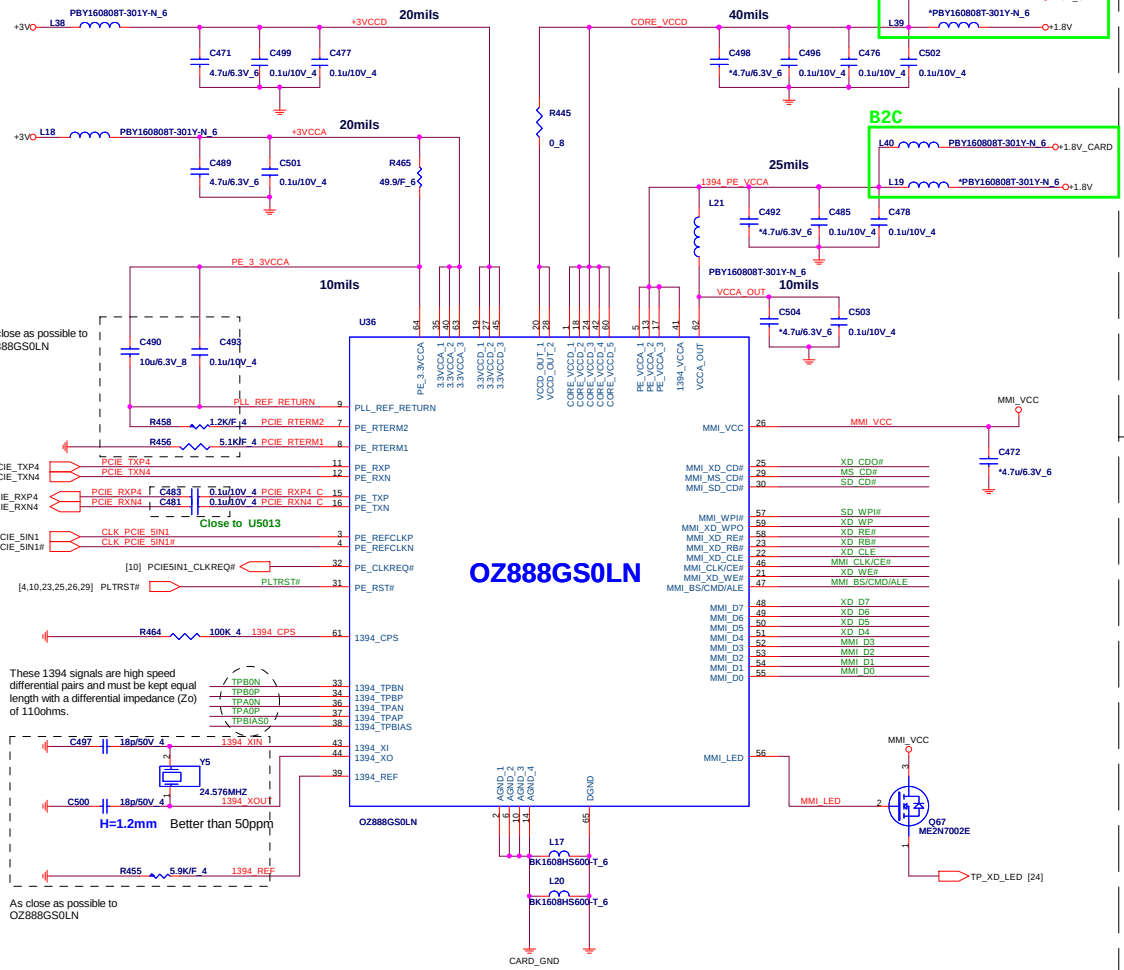
Vout=1.25[1+(52.3/100)]=1.903V



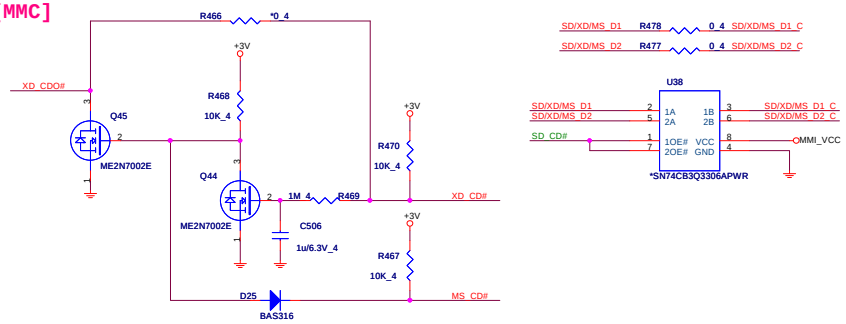
OZ888GS0LN

[MMC]

Each power pin is 100mA

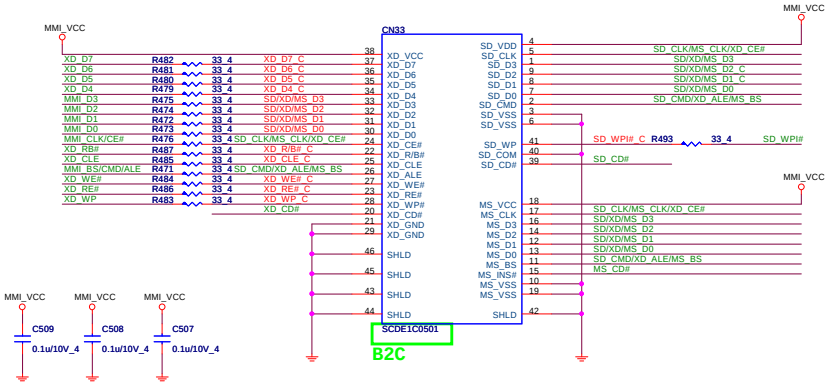


[MMC]



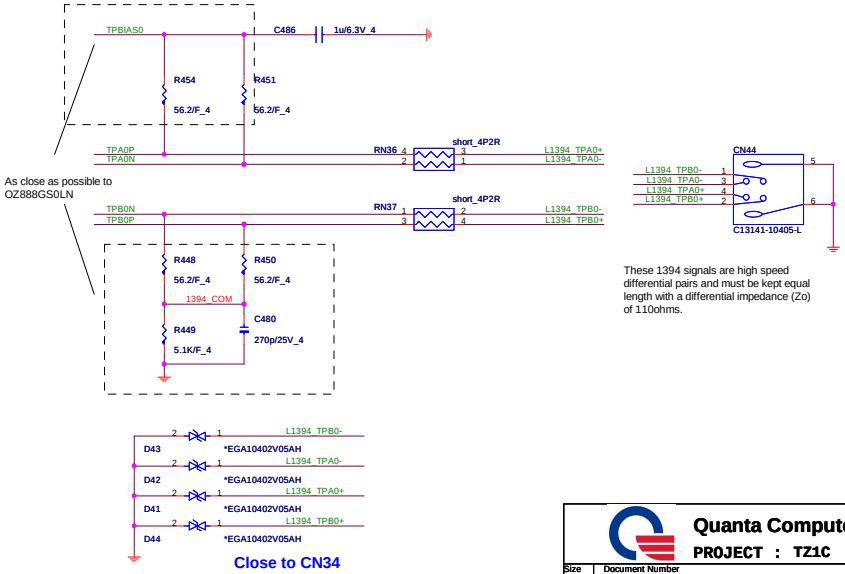
5 IN 1 CARD READER

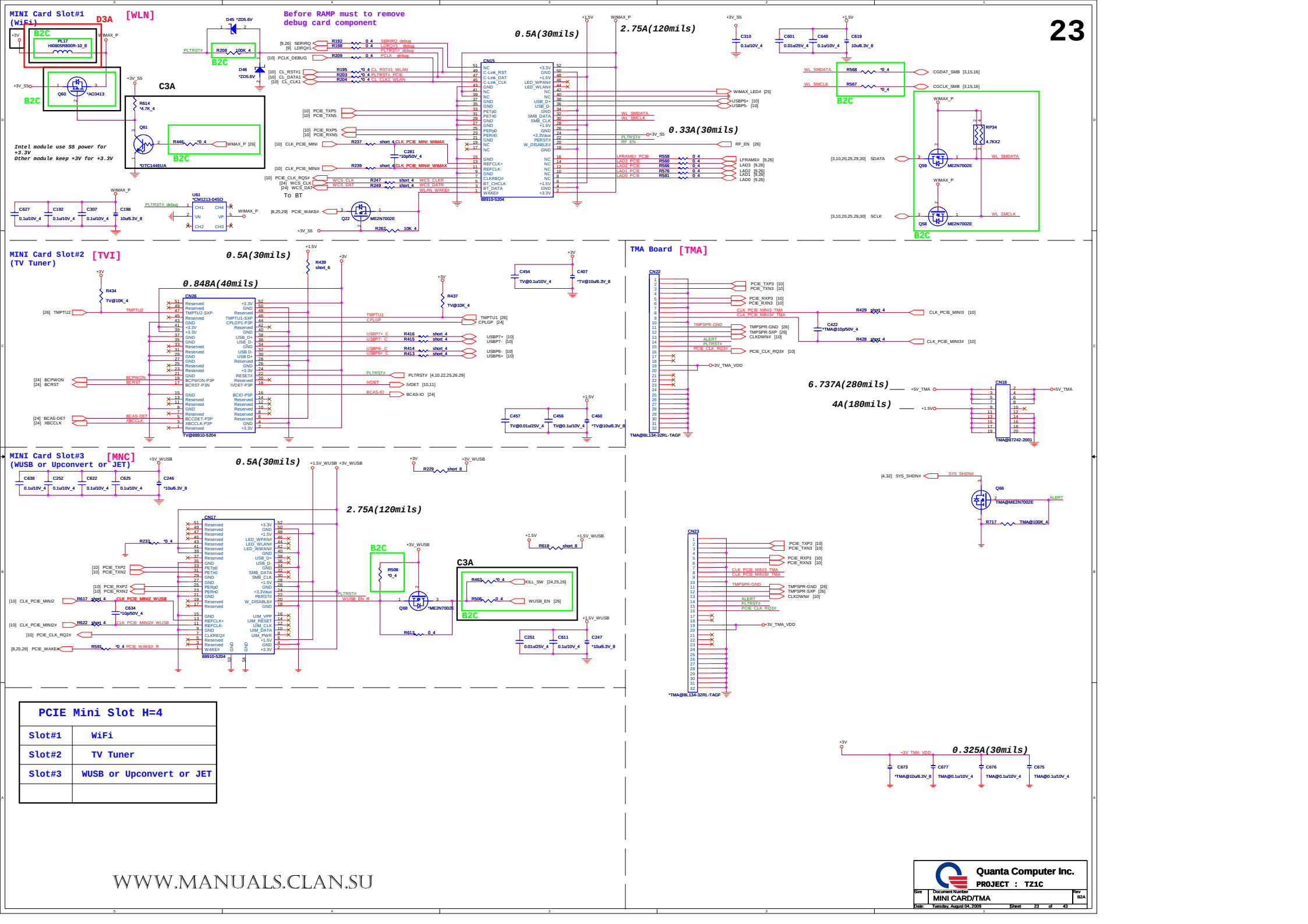
[MMC]



1394

[FIW]





PCIE Mini Slot H=4	
Slot#1	WiFi
Slot#2	TV Tuner
Slot#3	WUSB or Upconvert or JET

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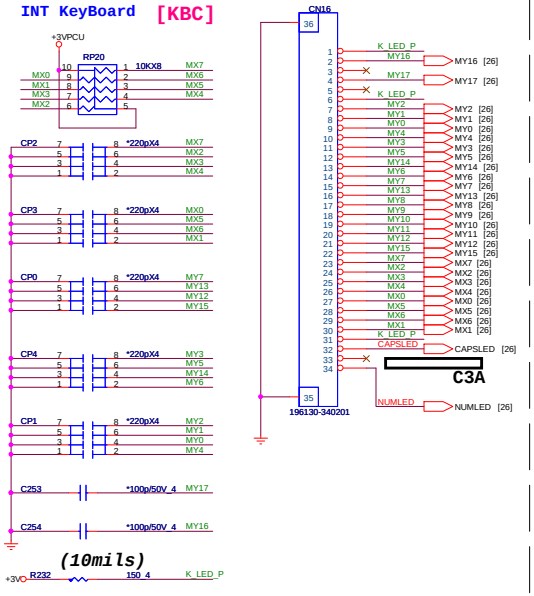
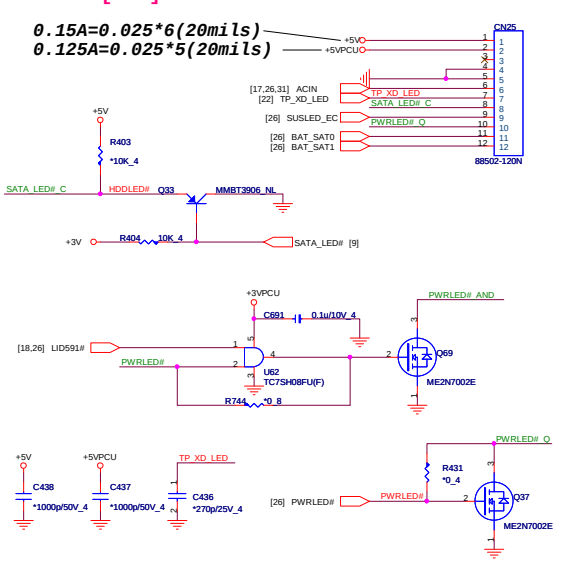
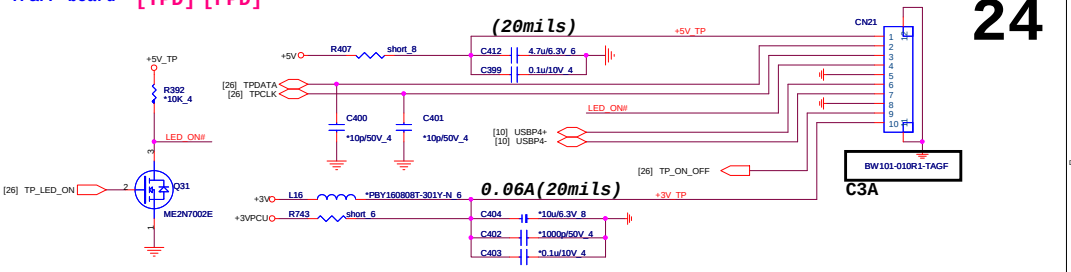
INT KeyBoard [KBC]



LED board [LED]

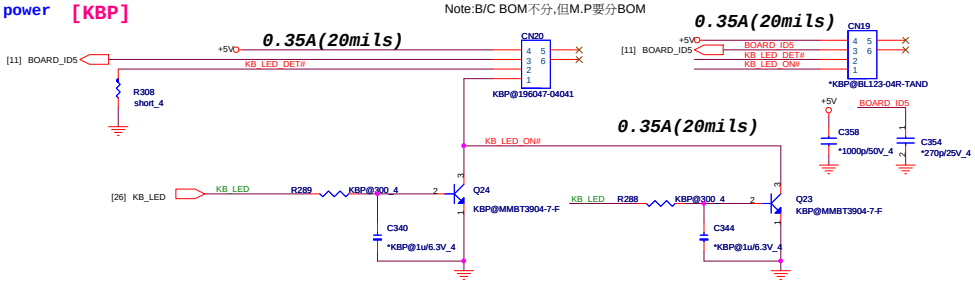


TP&FP board [TPD] [FPD]

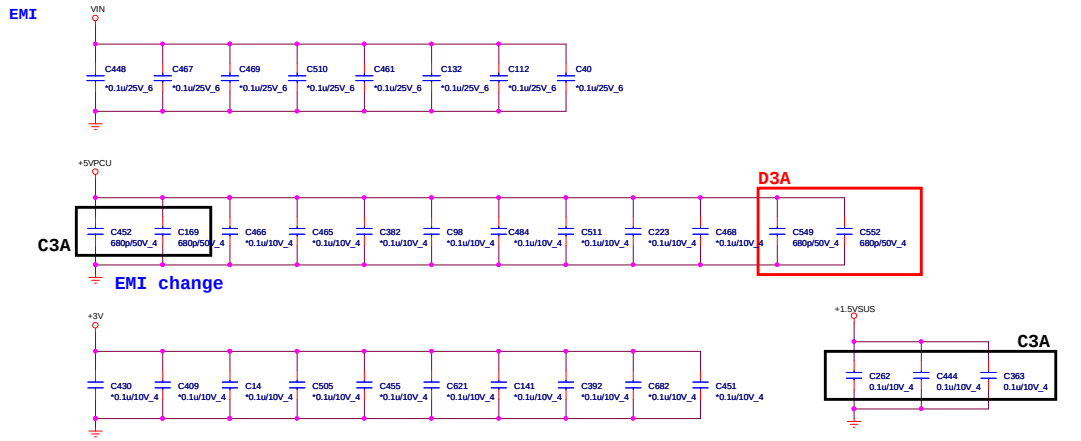


K/B LED power [KBP]

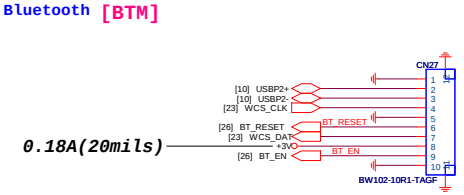
Note:B/C BOM不分,但M.P要分BOM



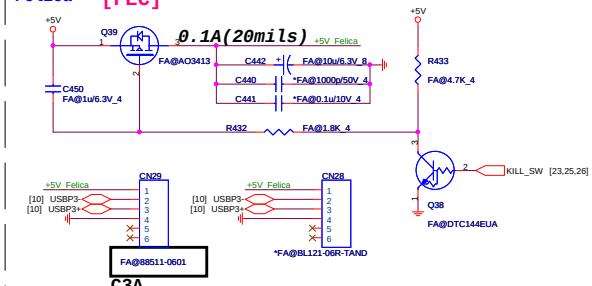
EMI



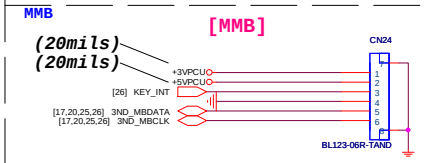
Bluetooth [BTM]



Felica [FEC]

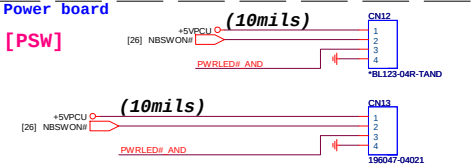


MMB [MMB]

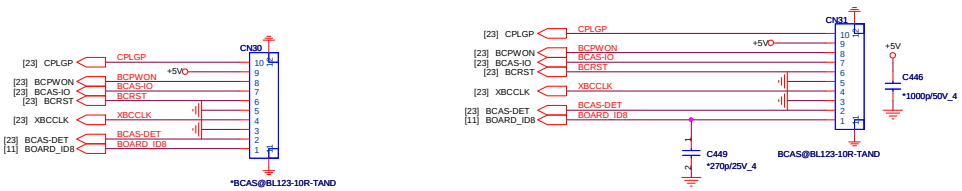


EMI

Power board [PSW]



B-CAS [BCS]



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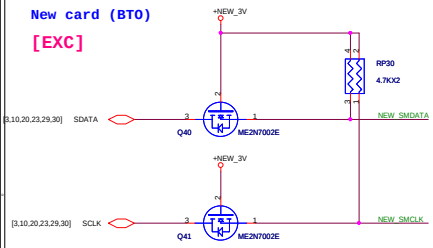
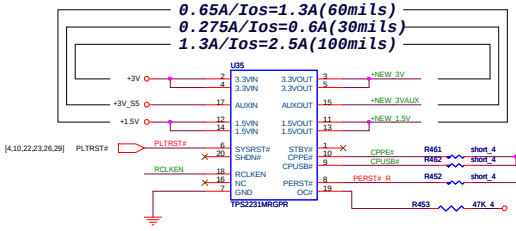
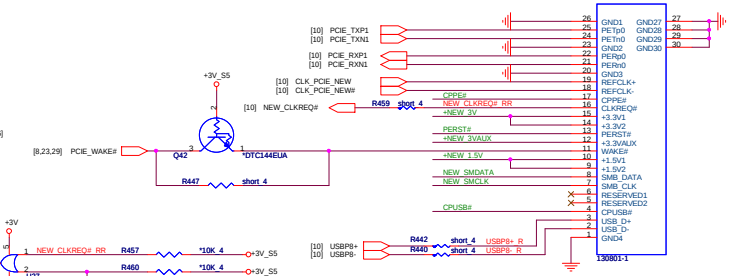
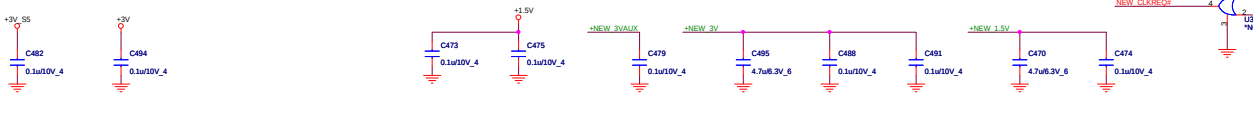
New card (BTO) [EXC]



0.65A/Ios=1.3A(60mils)
0.275A/Ios=0.6A(30mils)
1.3A/Ios=2.5A(100mils)

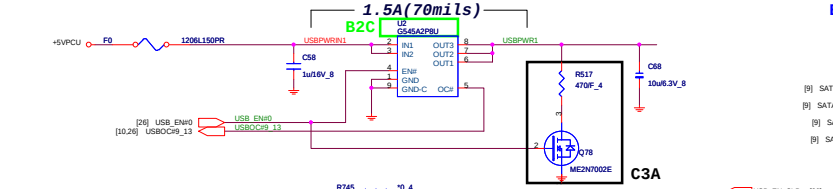




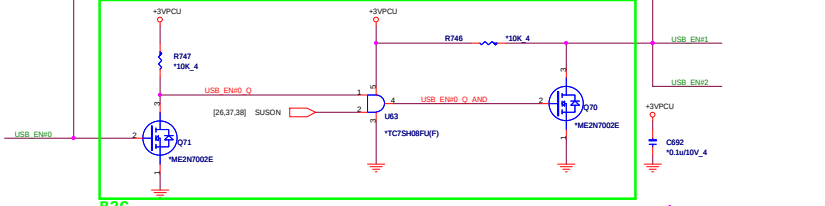


E-SATA [ESA]

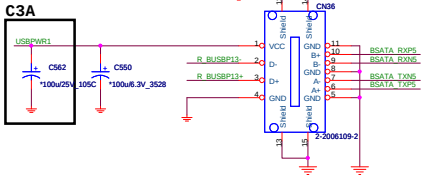
1.5A(70mils)



C3A

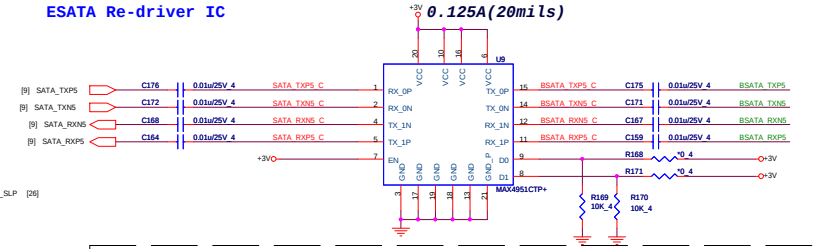


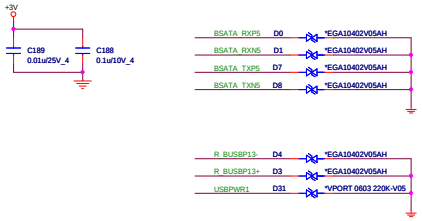
C3A



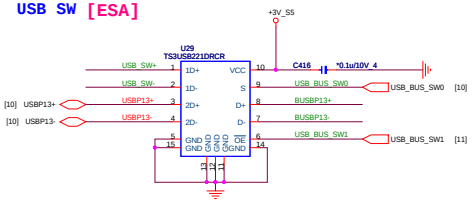
ESATA Re-driver IC

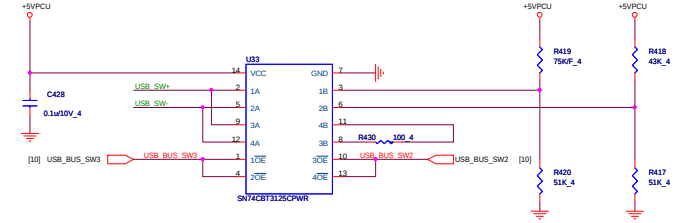
0.125A(20mils)

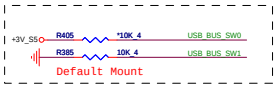




USB SW [ESA]







S	OE#	Function
X	H	Disconnect
L	L	D=1D
H	L	D=2D

OE#	Function
H	Disconnect
L	A port= B port

OE#	10E#	20E#	30E#	40E#
Mode3	High	High	Low	Low
Mode4	Low	Low	High	High

RF LED [LED]

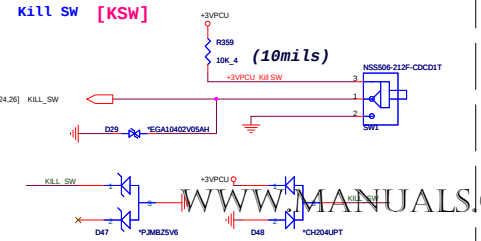
(10mils)

WIMAX LED [LED]

(10mils)

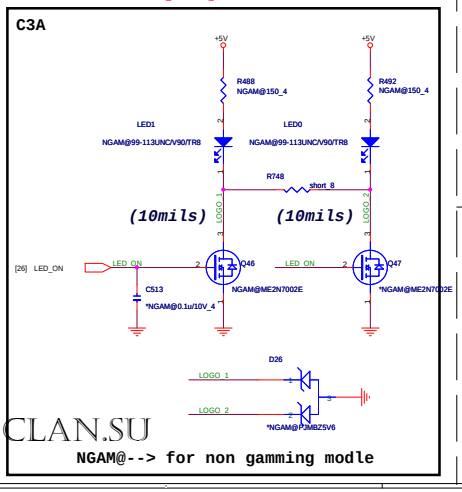
Kill SW [KSW]

(10mils)

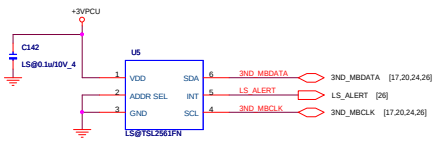


Satellite LED [LED]

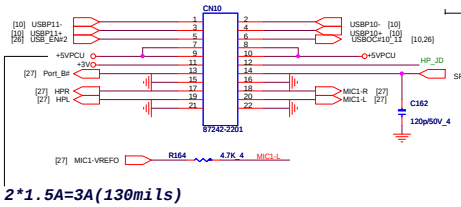
C3A



Light Sensor [LSR]



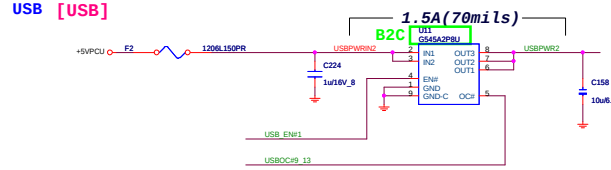
Audio&USB board [USB][ADO]

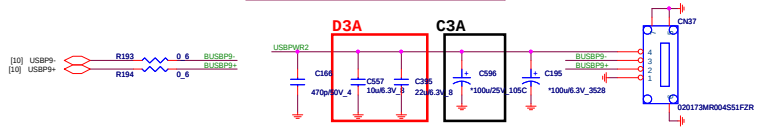


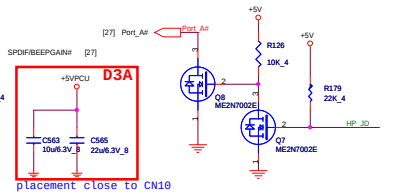
2*1.5A=3A(130mils)

USB [USB]

1.5A(70mils)







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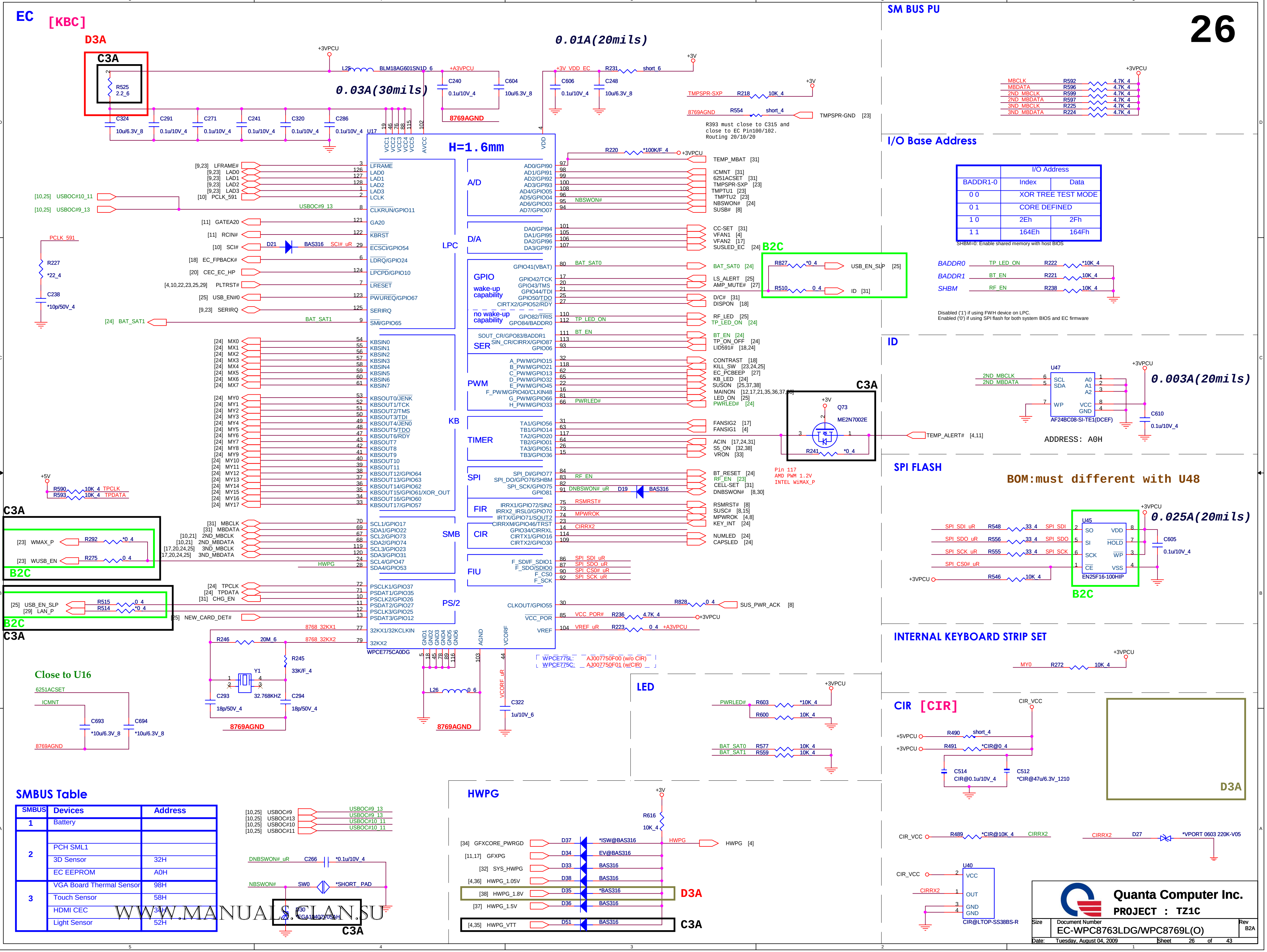
EC [KBC]



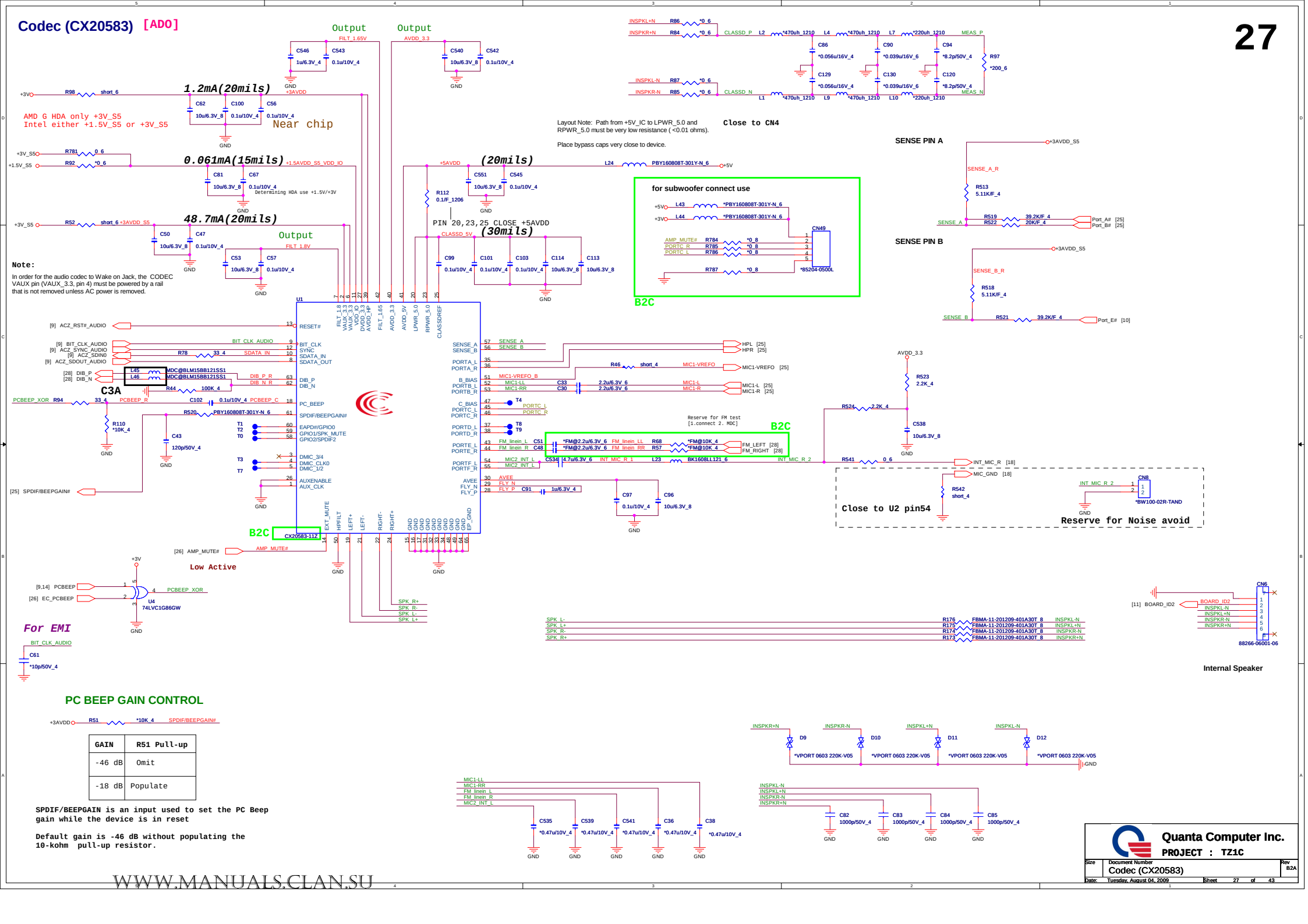
BADDR1-0	I/O Address: Index	Data
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

SHBM=0: Enable shared memory with host BIOS

SMBUS Table

SMBUS	Devices	Address
1	Battery	
2	PCH SML1	
	3D Sensor	32H
	EC EEPROM	A0H
3	VGA Board Thermal Sensor	98H
	Touch Sensor	58H
	HDMI CEC	34H
	Light Sensor	52H

Codec (CX20583) [ADO]



GAIN	R51 Pull-up
-46 dB	Omit
-18 dB	Populate

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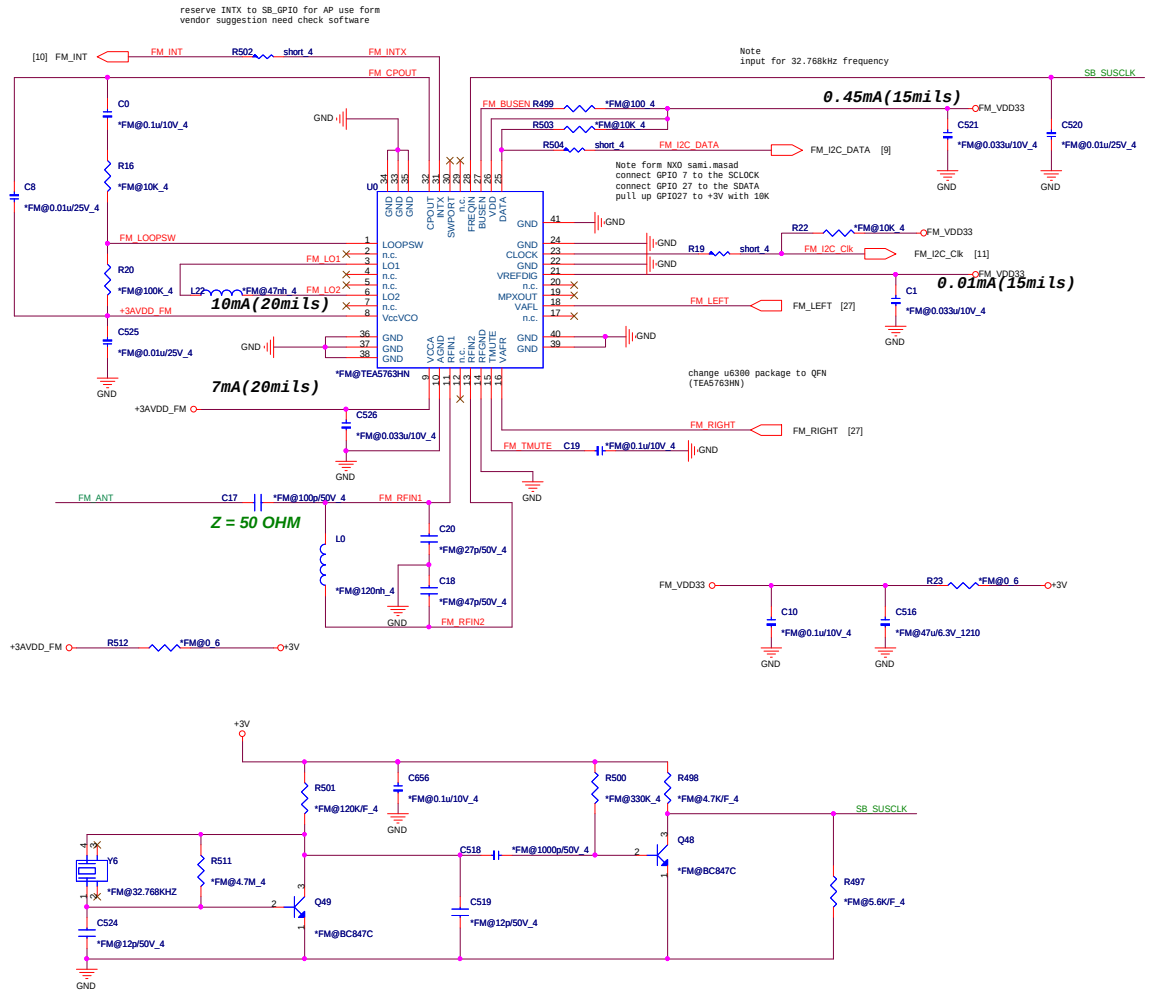
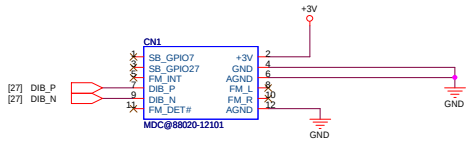
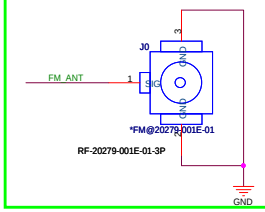
FM Tuner [FMM]

B2C



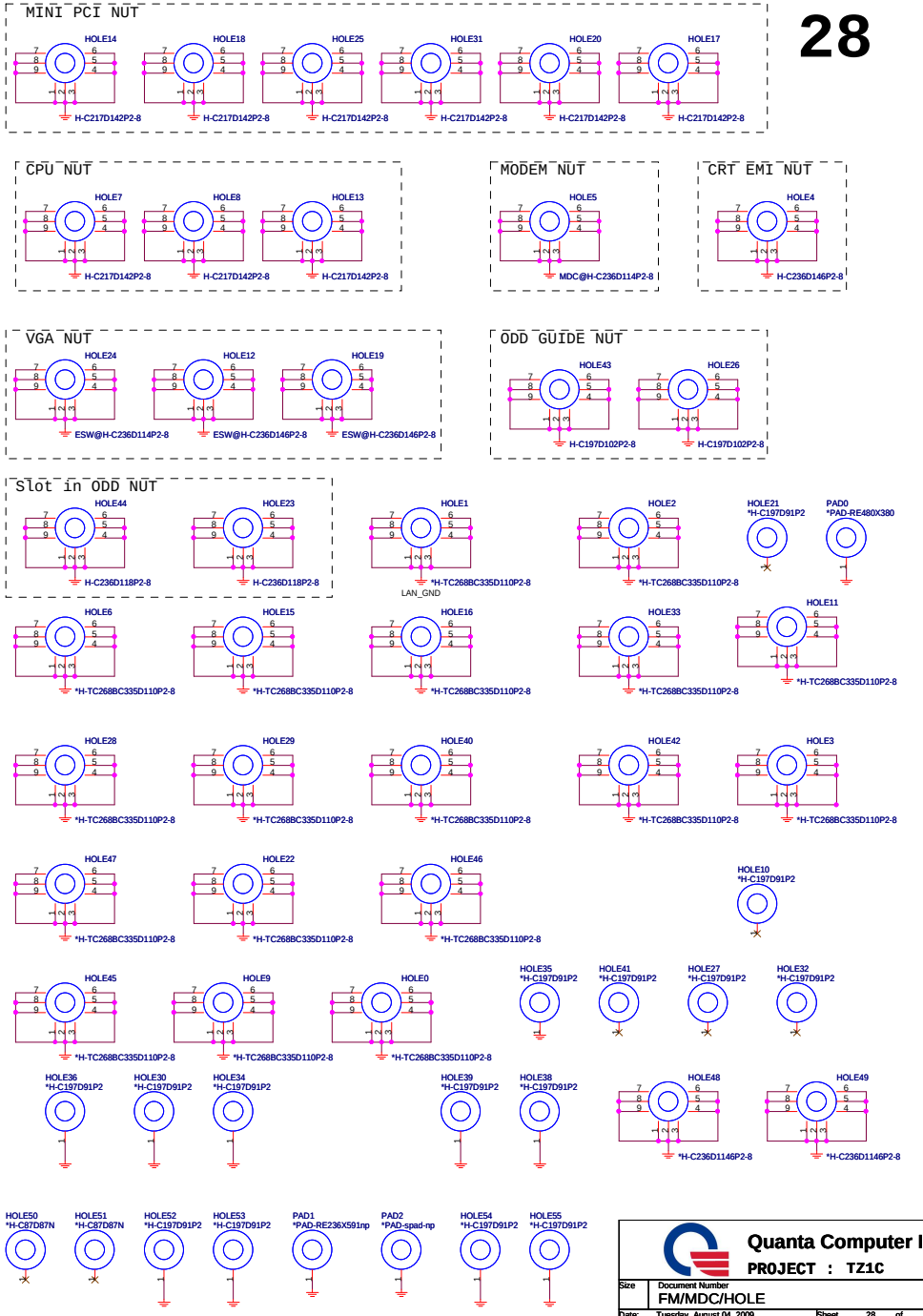
MDC [MDM]





B2C

HOLE



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Quanta Computer Inc.

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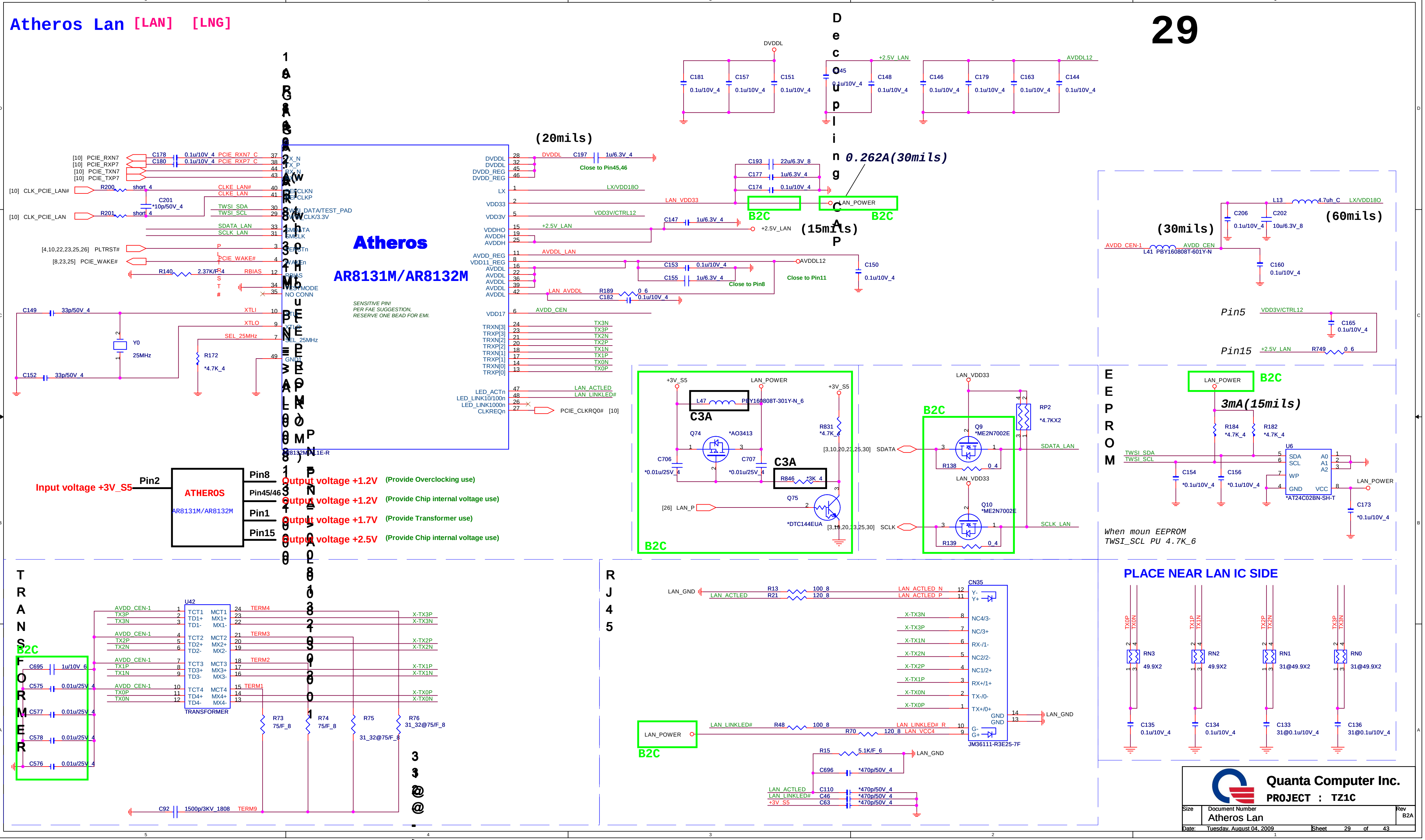
Atheros Lan [LAN] [LNG]



BRAIDWOOD

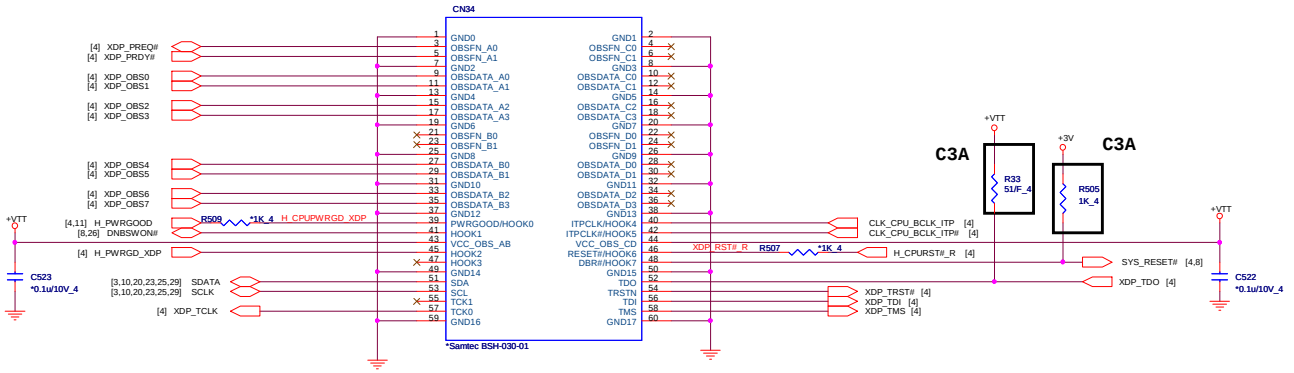
[BRD]

Feature Set	SKU Name (S)				
	Q57	H57	H55	P55	P57
BraidWood	Y	Y	N	N	Y

B2C

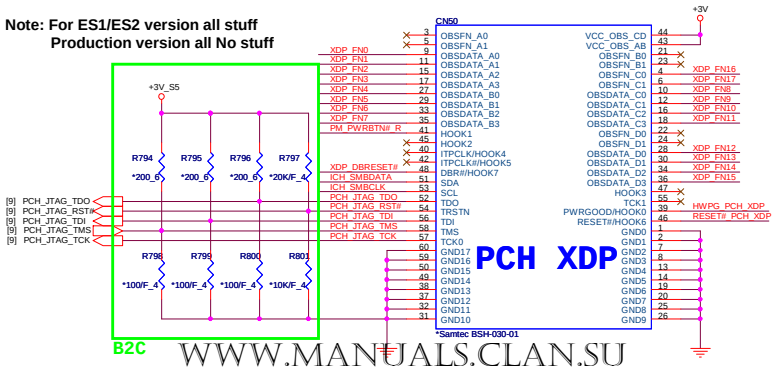
D3A

CPU XDP

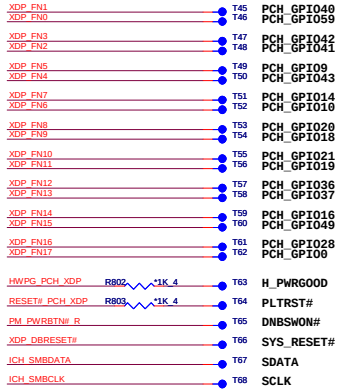


PCH XDP

Note: For ES1/ES2 version all stuff
Production version all No stuff



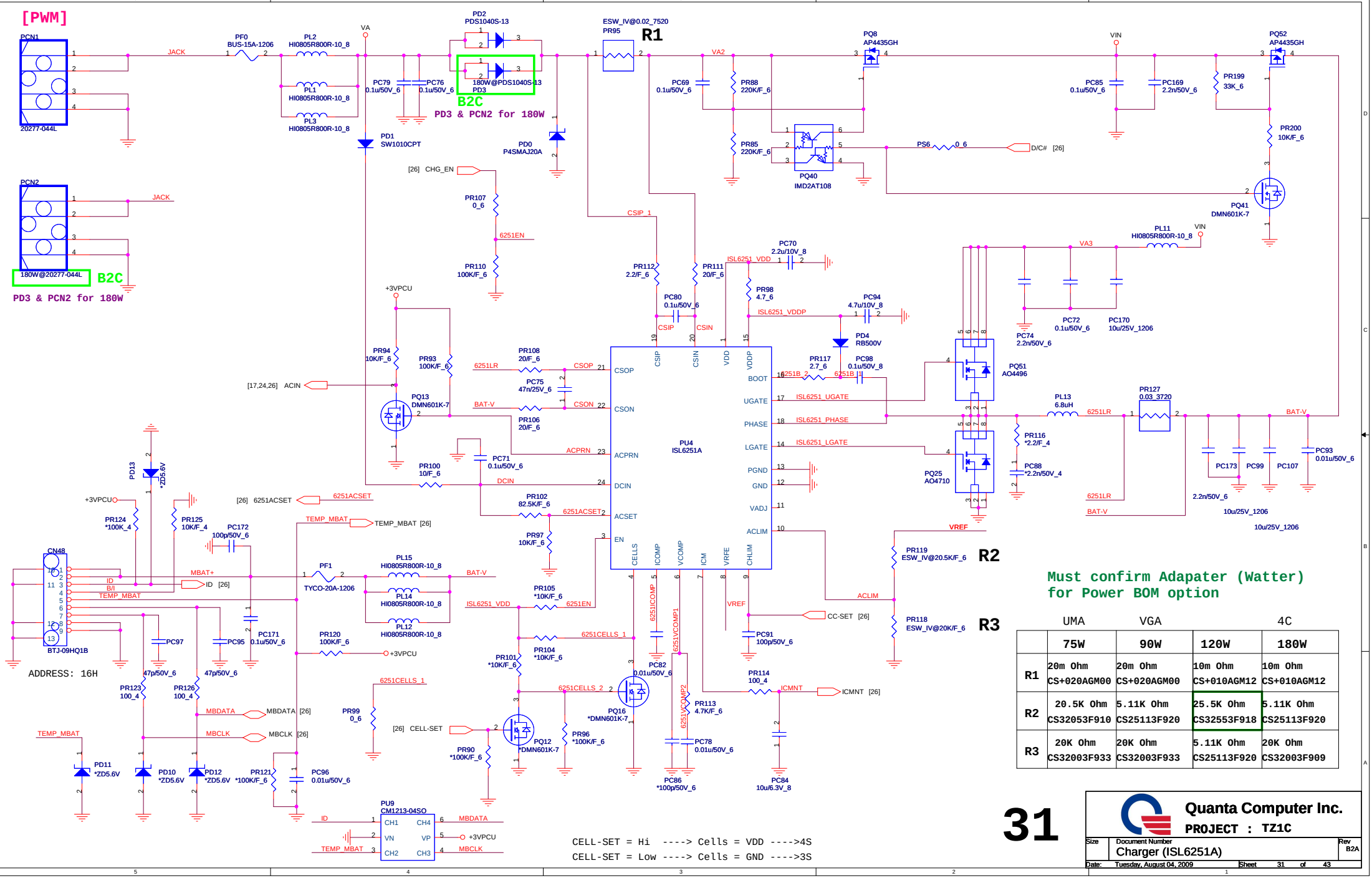
B2C



Quanta Computer Inc.
PROJECT : TZ1C

Size	Document Number	Rev
	NVRAM Connector	B2A

Date: Tuesday, August 04, 2009 Sheet 30 of 43



	UMA	VGA	4C	
	75W	90W	120W	180W
R1	20m Ohm CS+020AGM00	20m Ohm CS+020AGM00	10m Ohm CS+010AGM12	10m Ohm CS+010AGM12
R2	20.5K Ohm CS32053F910	5.11K Ohm CS25113F920	25.5K Ohm CS32553F918	5.11K Ohm CS25113F920
R3	20K Ohm CS32003F933	20K Ohm CS32003F933	5.11K Ohm CS25113F920	20K Ohm CS32003F909

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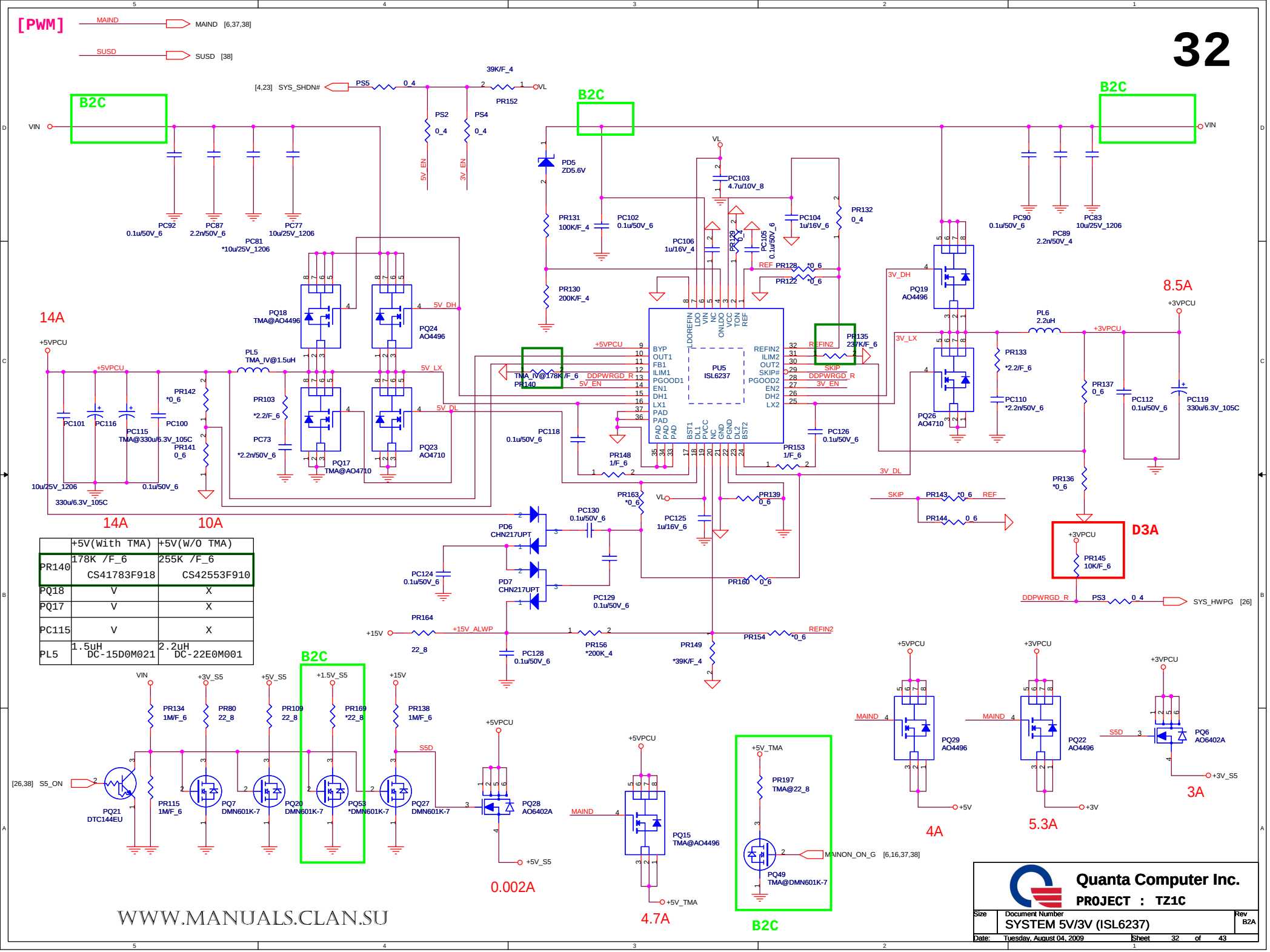
Quanta Computer Inc.
PROJECT : TZ1C

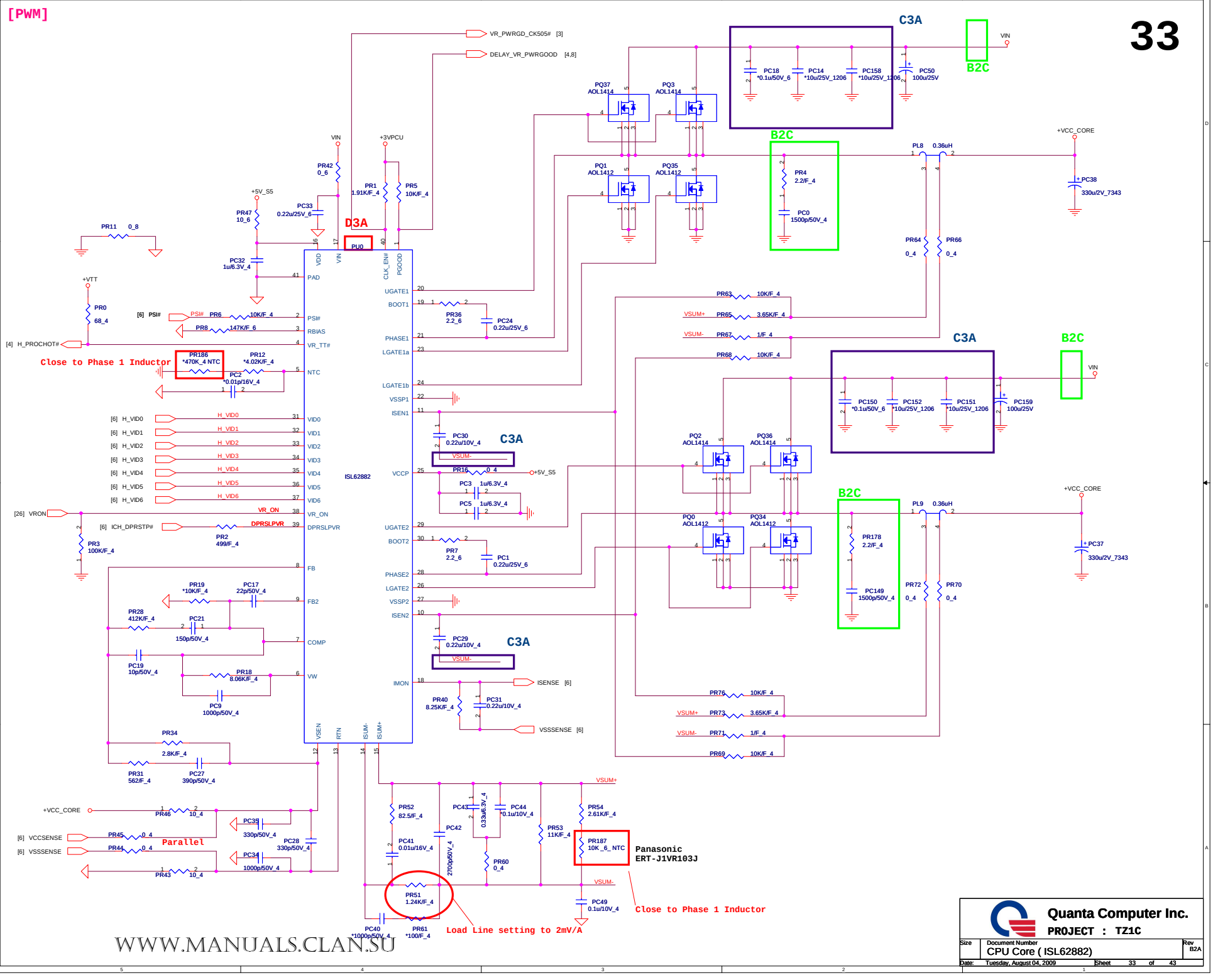
Size	Document Number	Rev
	Charger (ISL6251A)	B2A
Date: Tuesday, August 04, 2009	Sheet 31 of 43	



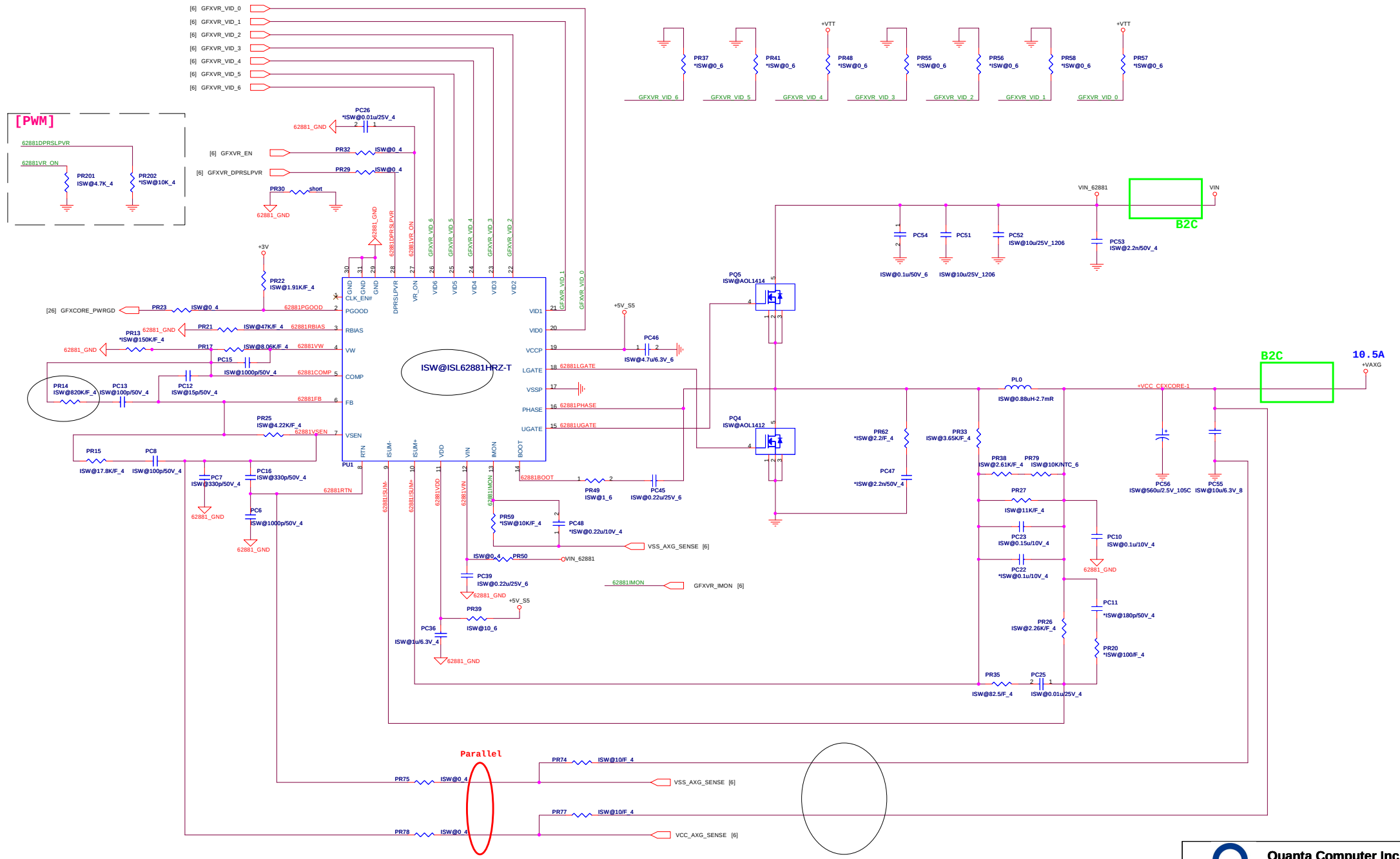
	+5V(With TMA)	+5V(W/O TMA)
PR140	178K /F_6 CS41783F918	255K /F_6 CS42553F910
PQ18	V	X
PQ17	V	X
PC115	V	X
PL5	1.5uH DC-15D0M021	2.2uH DC-22E0M001

Quanta Computer Inc.
PROJECT : TZ1C

Size	Document Number	Rev
	SYSTEM 5V/3V (ISL6237)	B2A
Date: Tuesday, August 04, 2009	Sheet 32 of 43	



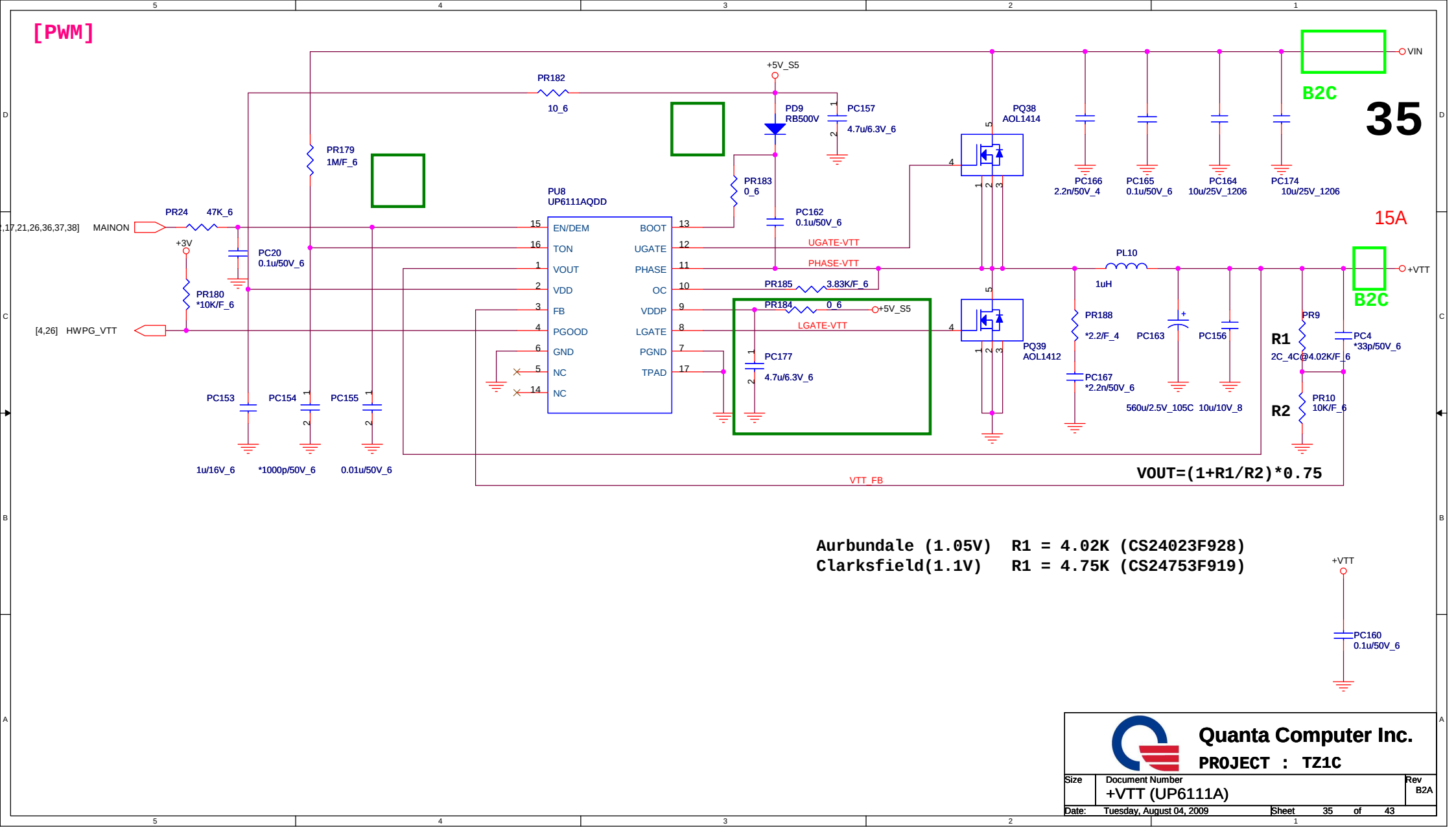
Quanta Computer Inc.		
PROJECT : TZ1C		
Size	Document Number: CPU Core (ISL6282)	Rev: B2A
Date: Tuesday, August 04, 2009	Sheet 33 of 43	

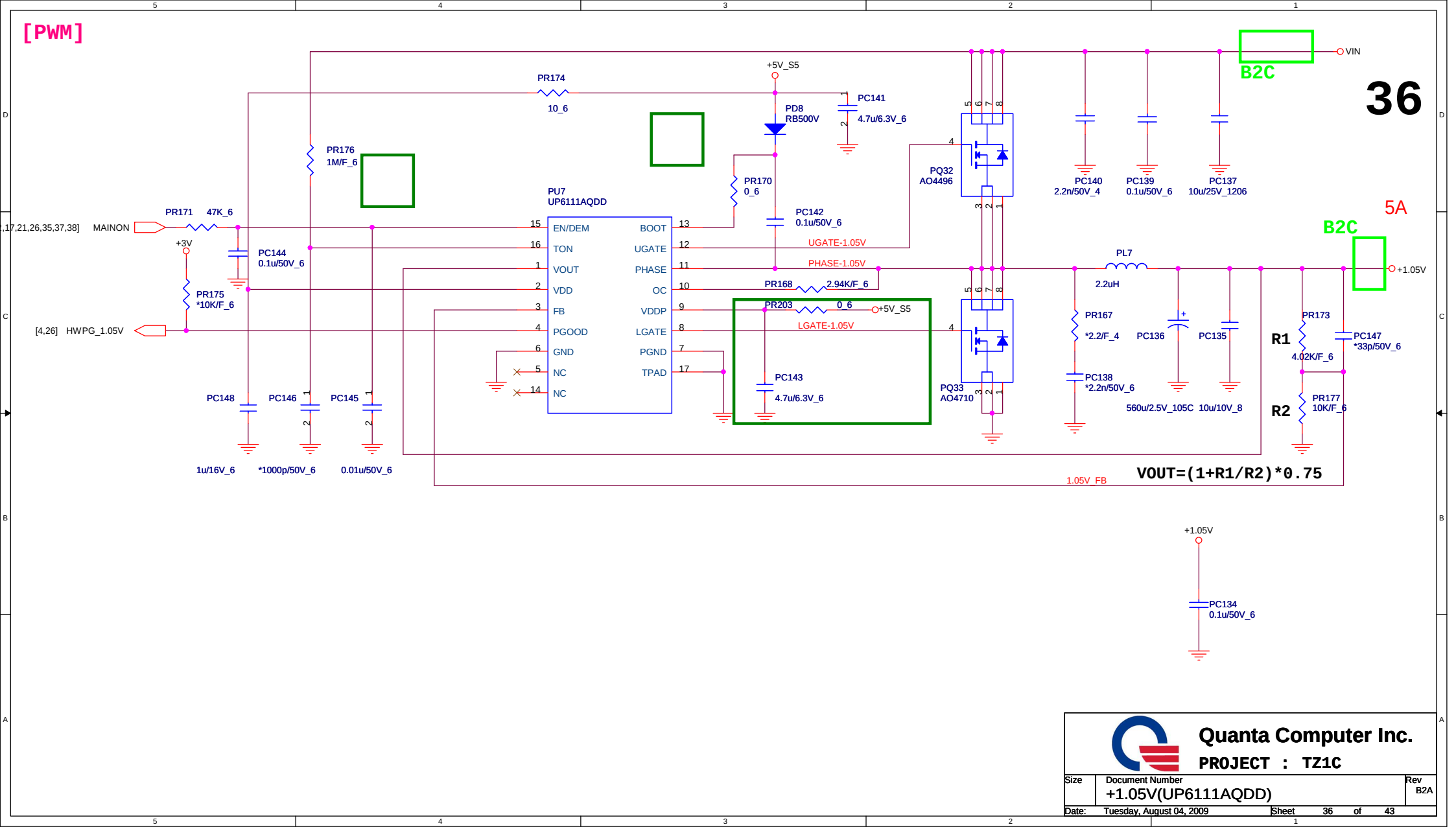


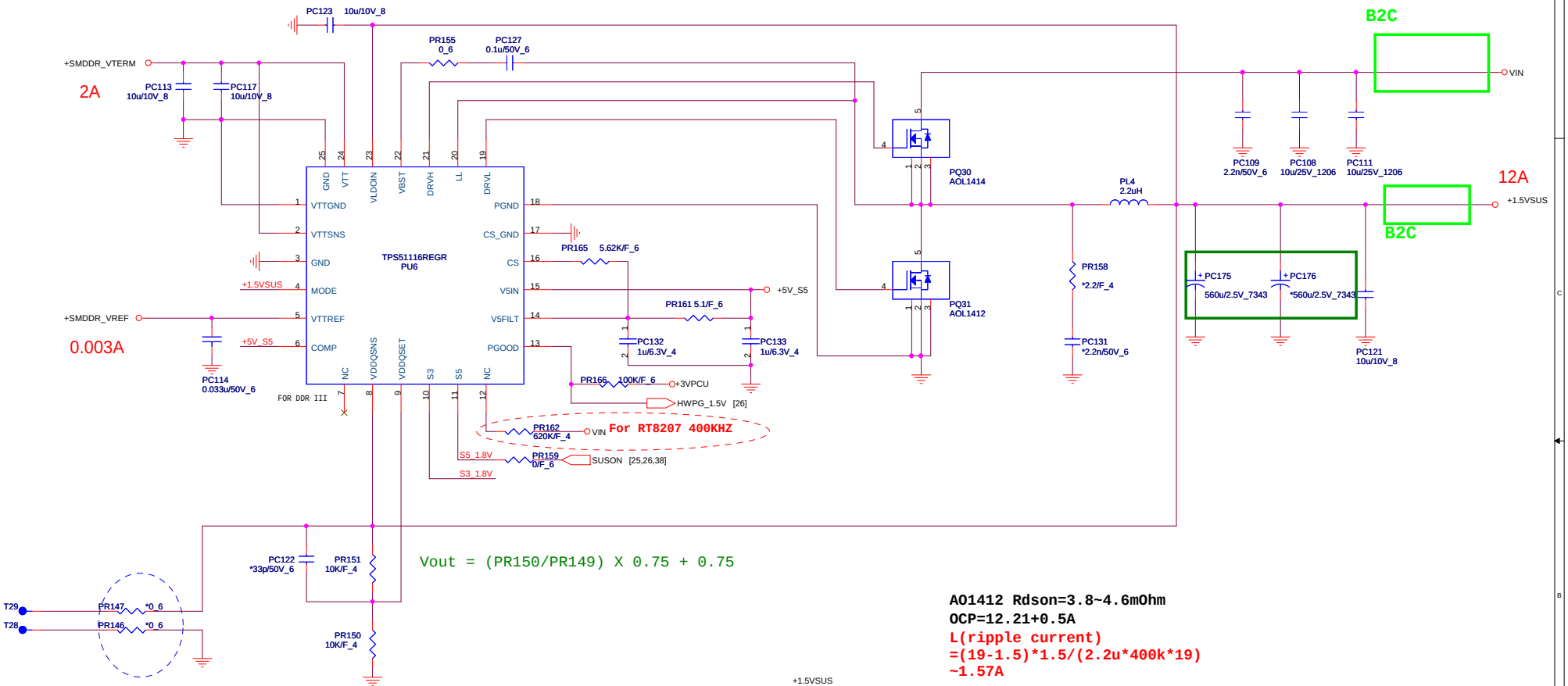
1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

Quanta Computer Inc.
PROJECT : TZ1C

Size	Document Number	Rev
	VAXG (ISL62881)	B2A
Date: Tuesday, August 04, 2009	Sheet 34 of 43	



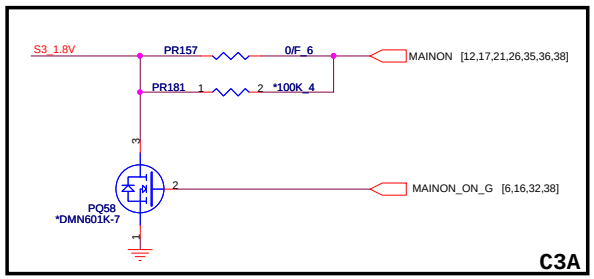


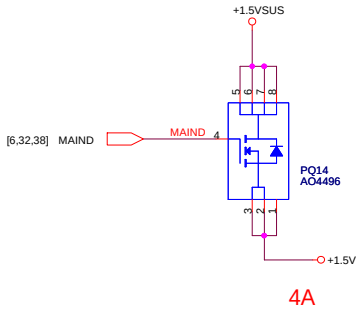


AO1412 Rdson=3.8~4.6mOhm
OCP=12.21+0.5A
L(ripple current)
=(19-1.5)*1.5/(2.2u*400k*19)
~1.57A

4.6m*12=RILIM*10uA
RILIM=5.62K

(10u*PR35)/Rdson+Delta_I/2=Iocp

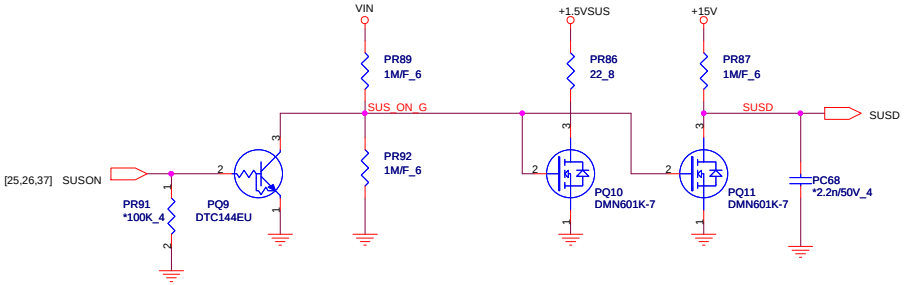




Quanta Computer Inc.
PROJECT : TZ1C

Size	Document Number	Rev
	DDR 1.5V(TPS51116)	B2A
Date: Tuesday, August 04, 2009	Sheet 37 of 43	

[PWM]



D3A

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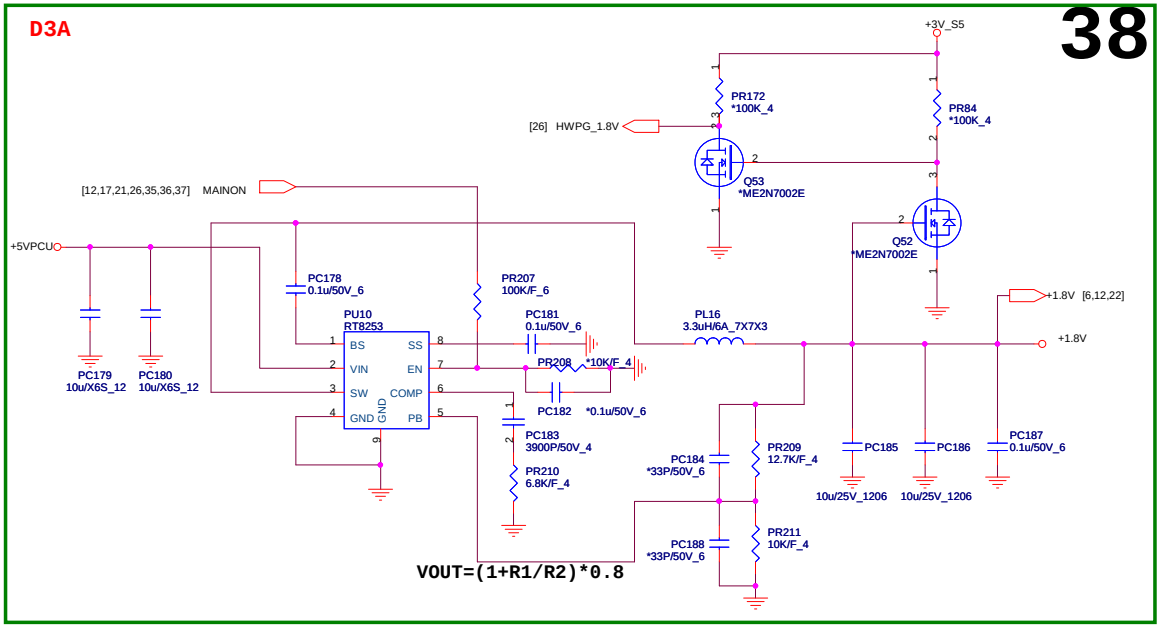
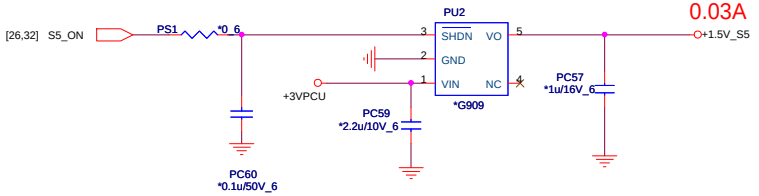
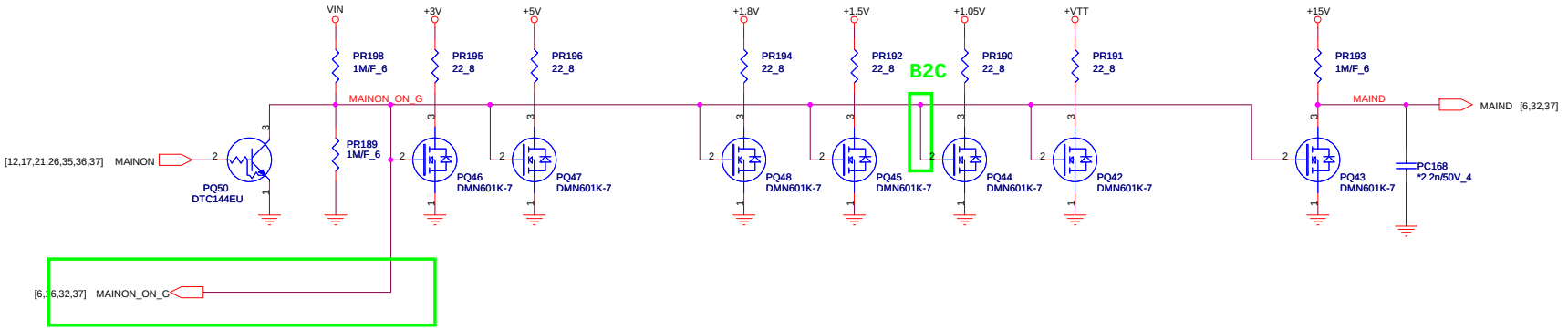


0.03A

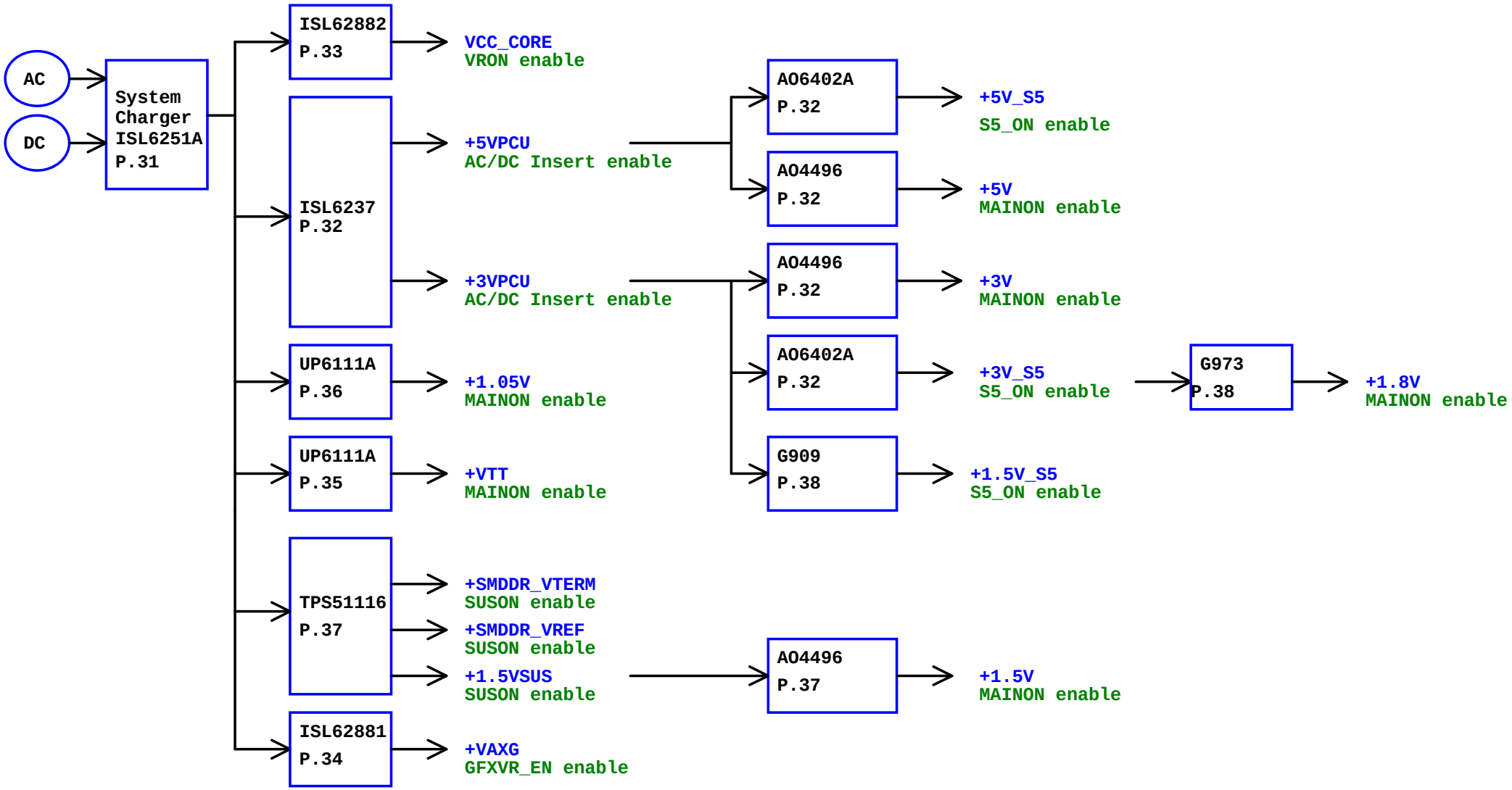




Quanta Computer Inc.

PROJECT : TZ1C

Size	Document Number	Rev
	Discharge (1.5V_S5/1.8V)	B2A
Date: Thursday, August 06, 2009	Sheet 38 of 43	



Quanta Computer Inc.
PROJECT : TZ1C

Size	Document Number	Rev
	POWER TREE TABLE	B2A

Date: Tuesday, April 07, 2009 Sheet 39 of 43

PCH POWER PLANE

LOGIC	SUPPLY	LEVEL	S0	S3	S4	S5
Fast Flash	VccpNAND	+1.8V/+3.3V	ON	OFF	OFF	OFF
Core	DcpSusByp	+1.05V	ON	OFF	OFF	OFF
CPU	V_CPU_IO	+VTT	ON	OFF	OFF	OFF
PCI	V5REF	+5V/+3V	ON	OFF	OFF	OFF
USB	V5REF_Sus	+5V_S5/+3V_S5	ON	ON	ON	ON
DisplayPort, SATA, PCI	VCC3_3	+3V	ON	OFF	OFF	OFF
Core	VccCore	+1.05V	ON	OFF	OFF	OFF
PCIE/DMI	VccDMI	+VTT/+1.05V	ON	OFF	OFF	OFF
Fast Flash	VccME3_3	+3V	ON	OFF	OFF	OFF
PCIE/DMI,SATA,USB	VccIO	+1.05V	ON	OFF	OFF	OFF
Core	VccLAN	+1.05V	ON	OFF	OFF	OFF
Core	VccME	+1.05V	ON	OFF	OFF	OFF
RTC	VccRTC	+VCCRTC	ON	ON	ON	ON
USB&PCI	VccSus3_3	+3V_S5	ON	ON	ON	ON
IntelR HD Audio	VccSusHDA	+1.5V_S5	ON	ON	ON	ON
Core	VccVRM	+V1.5S_1.8S	ON	OFF	OFF	OFF
CLK	VccAClk	+1.05V	ON	OFF	OFF	OFF
CRT	VccADAC	+3V	ON	OFF	OFF	OFF
DPLL	VccADPLLA	+1.05V	ON	OFF	OFF	OFF
DPLL	VccADPLLB	+1.05V	ON	OFF	OFF	OFF
PCIe/DMI	VccapllEXP	+1.05V	ON	OFF	OFF	OFF
IntelR FDI	VccFDIPLL	+1.05V	ON	OFF	OFF	OFF
SATA	VccSATAPLL	+1.05V	ON	OFF	OFF	OFF
Display	VccTX_LVDS	+1.8V	ON	OFF	OFF	OFF

Quanta Computer Inc.

PROJECT : TZ1C

Size	Document Number	Rev
	PCH POWER PLANE	B2A

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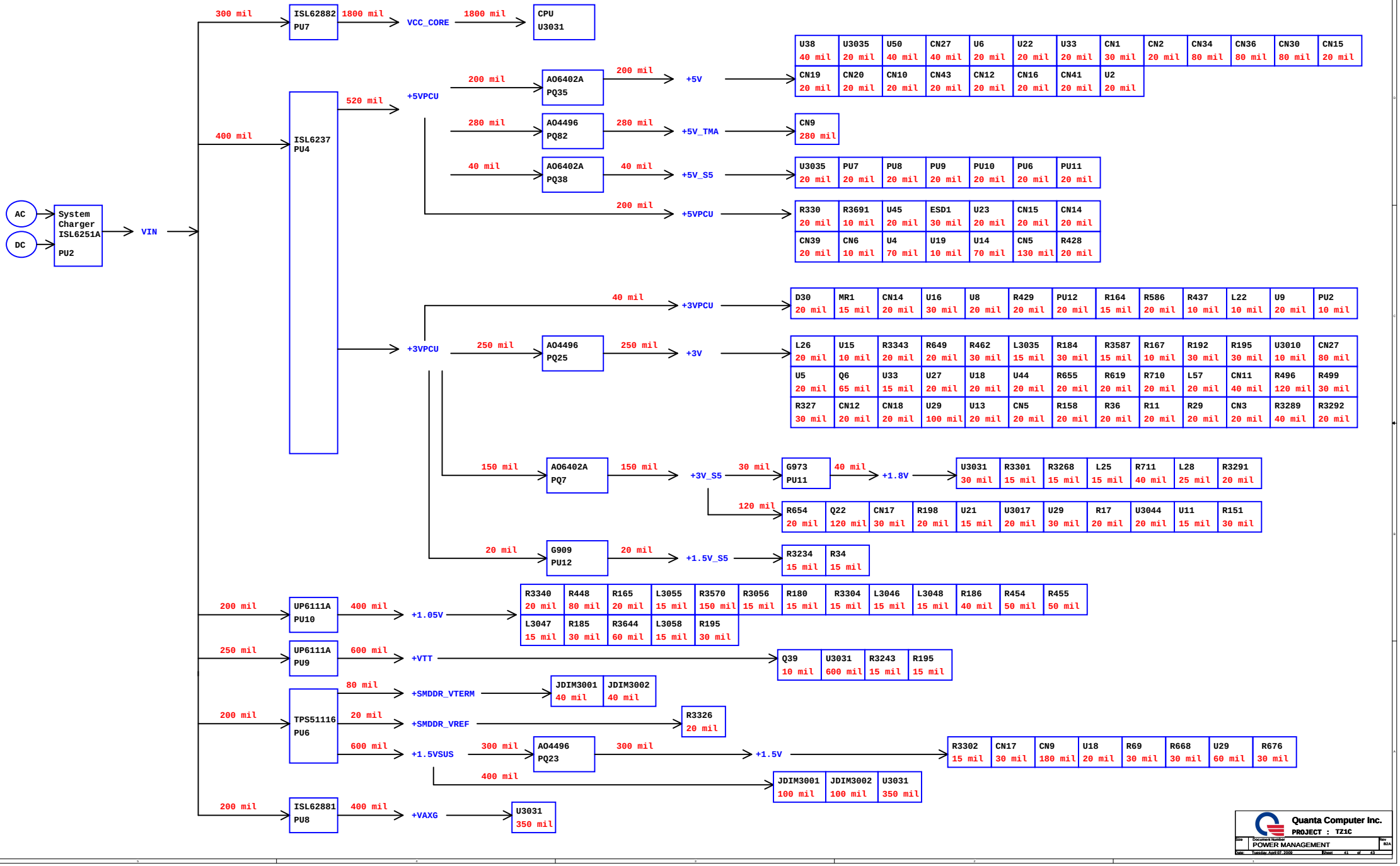

Model	REV	DATE	Change List	NOTE
TZ3	B2A	0223	First Release	

Quanta Computer Inc.
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Size	Document Number	Rev
	Change List	B2A

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Model	REV	DATE	Change List	NOTE
TZ3	B2C	0526	CPU FAN CONNECTOR 改側插,BW100-03R-TAND	BOM Change
			R664value change to IV,R676 change to EV	BOM Change
			Add R707,R389,R360,R690,R652 and reserve to PD	Schematic Change
			R254,R256 Change P/N CS05602FB15	BOM Change
			Change 396/HDMI@10K_4,R382/HDMI@10K_4) to (R396/HM@10K_4,R382/HM@10K_4)	BOM Change
			Add L14,R290,R278,R357,R398 power net name (VCCTX_LVDS)	Schematic Change
			Modify U43,CN42,JDIM0,JDIM1 Value to follow connector list	BOM Change
			VGA and TMA Fan共用,Value要改ESW_TMA@	BOM Change
			RN21改成ESW@	BOM Change
			Connector CN33 change Value and footprint	BOM Change
				Schematic Change
			CN35 change Value and footprint due to HI-POT fail	BOM Change
			C145,C148 connector to Lan IC power pin (+2.5V_LAN)	Schematic Change
			PCN2改ETMA@,EV+TMA時要上件	BOM Change
			PR14 change to CS48202FB00,PR28 change to CS44222FB14,PR51 change to CS21212FB18,Power's Value modify	BOM Change
			PQ44 Pin2 connect to Net MAINON_ON_G	Schematic Change
			Change Power P/N:CH21006JB10 CAP CHIP 1000P 50V(+-5%,X7R,0402) to CH21006KB16 CAP CHIP 1N 50V(+-10%,X7R,0402)	BOM Change
			Change Power P/N:CH61001ME96 CAP CHIP 10UF 6.3V(+-20%,X5R,0805) to CH6102K9A01 CAP CHIP 10U 10V(+-10%,X5R,0805)	BOM Change
			Change Power P/N:CH5101K9B01 CAP CHIP 1U 6.3V(+-10%,X5R,0402) to CH5102K9B06 CAP CHIP 1UF 10V (+-10%,X5R,0402)	BOM Change
			Change Power P/N:CH5471K9E07 CAP CHIP 4.7U 6.3V(+-10%,X5R,0603) to CH5471M9907 CAP CHIP 4.7U 6.3V(+-20%,X5R,0603)	BOM Change
			Change U53 from SLG8SP585V to SLG8SP585VTR	BOM Change
			Change PR28 original Value: 420K/F_4; P/N:CS44222FB14 to Value: 412K/F_4; P/N: CS44122FB00.	BOM Change
			Change PR34 original Value: 2.87K/F_4; P/N:CS22872FB10 to Value: 2.8K/F_4; P/N: CS22802FB02.	BOM Change
			Change PR51 original Value: 1.21K/F_4; P/N:CS21212FB18 to Value: 1.24K/F_4; P/N: CS21242FB20.	BOM Change
			Change PL8 and PL9 original Value: 0.36uH; P/N:CV+36F0MZ05 to Value: 0.36uH; P/N: CV+18V0MZ04.	BOM Change
			Delete PC40 Value: 1000p/50V_4; P/N:CH21006JB10 and PR61 Value: 100/F_4; P/N: CS11002FB22.	Schematic Change
			Change PR26 original Value: ISW@3.3K/F_4; P/N:CS23302FB12 to Value: ISW@2.26K/F_4; P/N: CS22262FB05.	BOM Change
			Change PR25 original Value: ISW@6.81K/F_4; P/N:CS26812FB13 to Value: ISW@4.22K/F_4; P/N: CS24222FB11.	BOM Change
			Delete PC11 Value: ISW@180p/50V_4; P/N: CH11806JB09 and PR20 Value: ISW@100/F_4; P/N: CS11002FB22.	Schematic Change
			Change PC84 original Value: 3.3n/100V_8; P/N: CH2338J0A04 to Value: 10u/6.3V_8; P/N: CH61001ME96.	BOM Change
			Change PR168 original Value: 5.76K/F_6; P/N: CS25763F916 to Value: 2.94K/F_6; P/N: CS22943F916.	BOM Change
			Change PR34 from CS22802FB02 to CS22802FB18	BOM Change
			Change CN40 BW100-03R-TAND (P/N DFWF03MS010) 臥式 to BW100-03S-TAND (P/N DFWF03MS000) 立式	BOM Change
			Change CN14 BW100-03S-TAND (P/N DFWF03MS000) 立式 to BW100-03R-TAND (P/N DFWF03MS010) 臥式	BOM Change
			Change C388 footprint CC0402-C to CC0402	footprint Change
			Change C394 footprint CC0402-C to CC0402	footprint Change
			Change C384 footprint CC0402-C to CC0402	footprint Change
			Change R794 from 200_4 RC0402 to 200_6 RC0603	footprint Change
			Change R795 from 200_4 RC0402 to 200_6 RC0603	footprint Change
			Change R796 from 200_4 RC0402 to 200_6 RC0603	footprint Change
			Change R794/R795/R796/R797/R798/R799/R800/R801 to *(default no stuff) for QS sample	Schematic Change
			Remove M2 and Add M3 (DDR3 VREF_DQ)	Schematic Change
			Change R477/R478 to *(default no stuff)	Schematic Change
			Change U38 from *SN74CB3Q3305 to SN74CB3Q3306APWR	Schematic Change
			Change (DGPU_EDID from GPIO21 to GPIO67) Add (R829 to GPIO21 and PD to GND)	Schematic Change
			Remove JP0 ~ JP13	Schematic Change
			WIMAX: R742,R568,R567 No stuff ; Q60,Q61,R614,RP34,Q59,Q58 stuff	Schematic Change
			LAN: Change LAN(sheet 29) Original Power +3V_S5 to LAN_Power Add Q74,Q75,R831(default NC), R830 (default stuff)	Schematic Change
			ROM Change U45 to EON(vender) for P/N different with U48	BOM Change
			Remove C685	Schematic Change
			PQ44 (Gate routing to MAINON_ON_G)	Schematic Change
			WIMAX: Add R466 for WIMAX power control(option with WUSB_EN-->EC/GPIO47) R742,R568,R567 stuff Q60,Q61,R614,R466,RP34,Q59,Q58 No stuff	Schematic Change
			WUSB: Add R463 and R506 for WUSB_EN control option between EC/GPIO47 and KILL_SW R463 no stuff	Schematic Change
			Change CLKDWN#(TMA) from (EC/GPIO27) to (PCH/GPIO64) and add R354 Pull hi to +3V Add LAN_P for LAN power control to EC/GPIO27	Schematic Change
			Add PR169,PQ53 for 1.5V_S5 discharge Change PR193,PQ49 value to TMA@	Schematic Change
			Add R510(No stuff) and R827(Stuff) connect SB_EN_SLP to EC/GPIO 44 [use to option support wake on mouse or not]	Schematic Change
			Add R514 and R515 Set USB_EN_SLP default to EC/GPIO27	Schematic Change
			for Layout request RP1/RP5/RP6/RP8/RP10/RP12/RP13/RP16/RP18 swap pin	Schematic Change
			change LAN transformer P/N: 10/100: PN=>DB0EF7LAN01 / DB0EL5LAN00 GIGA: PN=>DBBL5MLAN01	BOM Change
			change PR4/PC0/PR178/PC149 from no stuff to stuff	Schematic Change

Quanta Computer Inc.
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Size	Document Number	Rev
	Change List	B2A

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