ZT7121

3A, 6V Synchronous Step-Down DC/DC Converter

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■ This data sheet is subject to change without notice.

REVISION HISTORY

Rev.	Date
0.5	08.07.10
0.6	09.04.03

FEATURES

- 2.7V to 6V input voltage
- Output current up to 3A
- Output voltage adjustable 0.8V to 0.9×V_{IN}
- Efficiency up to 95%
- 1.5MHz fixed frequency switching
- Input synchronous frequency 1MHz to 2MHz
- Power good output
- Over current protection
- Over temperature protection
- Internal soft start
- RoHS Compliant and 100% Lead (Pb) Free

APPLICATIONS

- µP/ASIC/DSP/FPGA core and I/O supplies
- Printers and LCD TVs
- Network and telecom equipments
- Point of load regulators

ORDERING INFORMATION

PART	PACKAGE	RoHS	Ship, Quantity
ZT7121D	DFN 3x3-10L	Yes	Tape and Reel

DESCRIPTION

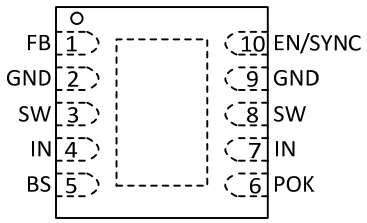
The ZT7121 is an internally compensated 1.5MHz fixed frequency PWM synchronous step-down regulator. It can input synchronous frequency from 1MHz to 2MHz. The ZT7121 operates from 2.7V to 6V input, the generated output can be as low as 0.8V and the output current can be up to 3A.

The ZT7121 integrates a 60mΩ high-side switch and a 60mΩ synchronous rectifier for high efficiency without an external Schottky diode. With peak current mode control and internal compensation, the ZT7121 based solution is with compact footprint and minimum external components.

The ZT7121 is available in the DFN 3x3-10L package, and it is RoHS compliant and 100% lead (Pb) free.

Pin Configurations

Top View
DFN 3x3-10L



Absolute Maximum Rating

IN, FB, EN/SYNC, POK to GND ..... –0.3V to +6.5V
SW to GND ..... –0.3V to V_{IN}+0.3V
BS to SW ..... –0.3V to +6.5V
Junction Temperature ..... 150°C
Lead Temperature ..... 260°C
Operating Temperature Range ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electro-Static Discharge Sensitivity

This integrated circuit can be damaged by ESD. It is recommended that all integrated circuits be handled with proper precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure.

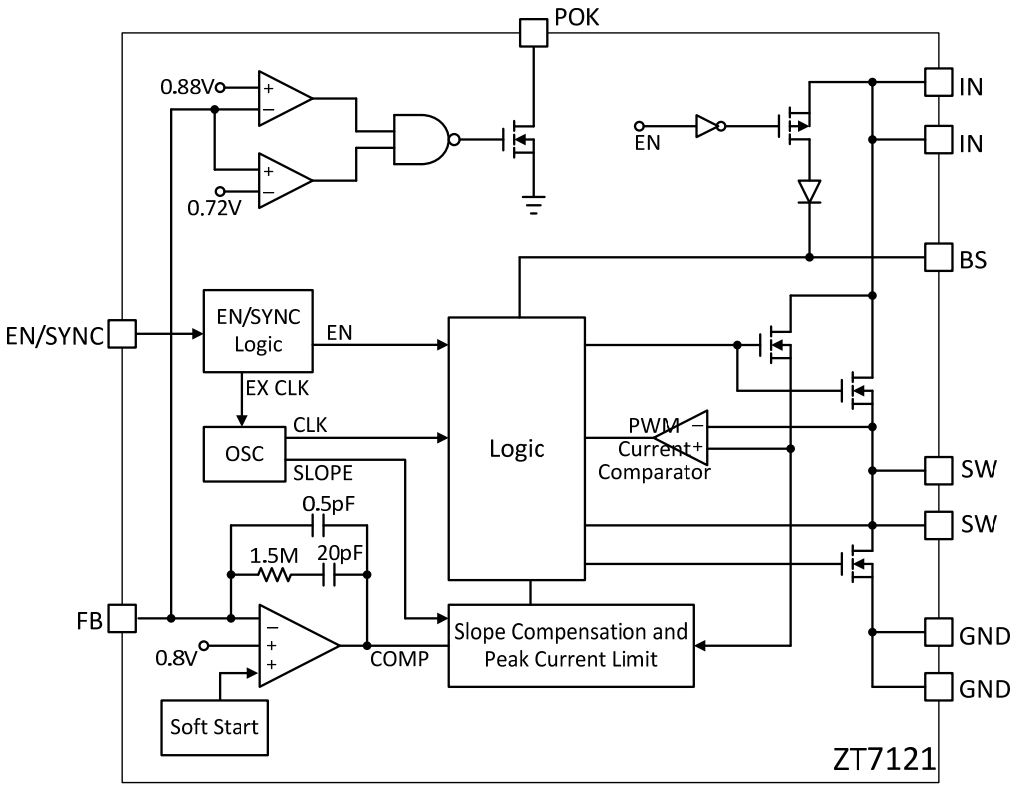
Package Thermal Characteristics

Thermal Resistance, θ_{JA}:
DFN 3x3-10L ..... 50°C/W
Thermal Resistance, θ_{JC}:
DFN 3x3-10L ..... 12°C/W

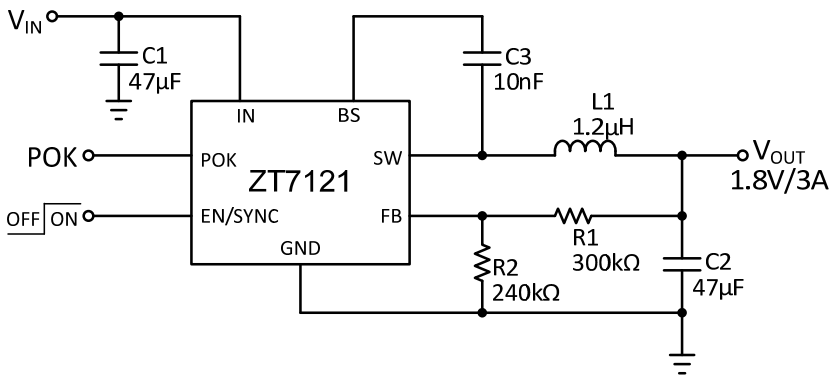
Pin Description

DFN 3x3-10L	Symbol	Description
1	FB	Feedback pin.
2, 9	GND	Ground pin.
3, 8	SW	Switch node connection to inductor.
4, 7	IN	Input supply pin.
5	BS	Bootstrap pin.
6	POK	Open drain power good output.
10	EN/SYNC	Enable and frequency synchronization input.

Functional Block Diagram



Typical Application Circuit



Electrical Specifications

(T_A = 25°C, V_{IN} = V_{EN} = +3.6V, unless otherwise noted.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage V_{IN}		2.7		6	V
Output Voltage V_{OUT}		0.8		0.9×V_{IN}	V
Supply Current	V_{EN} = V_{IN}, V_{FB} = 0.85V		750		µA
Shutdown Current	V_{EN} = 0V, V_{IN} = 6V		1		µA
IN Under Voltage Lockout Threshold	Rising edge		2.59	2.69	V
IN Under Voltage Lockout Hysteresis			200		mV
Regulated FB Voltage	T_A = 25°C	0.776	0.800	0.824	V
FB Input Current	V_{FB} = 0.85V		±50		nA
EN High Threshold	−40°C ≤ T_A ≤ +85°C	1.6			V
EN Low Threshold	−40°C ≤ T_A ≤ +85°C			0.4	V
Internal Soft Start Time			120		µs
High Side Switch On Resistance	I_{SW} = 300mA		60		mΩ
Low Side Switch On Resistance	I_{SW} = −300mA		60		mΩ
SW Leakage Current	V_{EN} = 0V, $V_{IN,}$ = 6V, V_{SW} = 0V or 6V	−10		10	µA
BS Under Voltage Lockout Threshold			1.8		V
High Side Switch Current Limit	Sourcing	4.0	4.5		A
Low Side Switch Current Limit	Sinking		3.5		A
Oscillator Frequency		1.2	1.5	1.8	MHz
Maximum Synchronous Frequency			2		MHz
Minimum Synchronous Frequency			1		MHz
Maximum Duty Cycle			90		%
POK Upper Trip Threshold	FB respect to the nominal value		10		%
POK Lower Trip Threshold	FB respect to the nominal value		−10		%
POK Output Voltage Low	I_{SINK} = 5mA			0.4	V
POK Deglitch Timer			30		µs
Thermal Shutdown Threshold	Hysteresis = 20°C		150		°C

APPLICATION INFORMATION

Pin Assignment

FB: Feedback. This is the input to the error amplifier. An external resistive divider connects this pin between the output and GND. The voltage on the FB pin compares to the internal 0.8V reference to set the regulation voltage.

GND: Ground. Connect these pins with larger copper areas to the negative terminals of the input and output capacitors.

SW: Switch Node Connection to the Inductor. These pins connect to the internal high and low-side power MOSFET switches. All SW pins must be connected together externally.

IN: Input Supply. A decoupling capacitor to ground is required close to these pins to reduce switching spikes.

BS: Bootstrap. A capacitor between this pin and SW provides a floating supply for the high-side gate driver.

POK: Open Drain Power Good Output. "HIGH" output indicates V_{OUT} is within ±10% window. "LOW" output indicates V_{OUT} is out of ±10% window. POK is pulled down in shutdown.

EN/SYNC: Enable and Frequency Synchronization Input Pin. Forcing this pin below 0.4V shuts down the part. Forcing this pin above 1.6V turns on the part. Applying a 1MHz to 2MHz clock signal to this pin synchronizes the internal oscillator frequency to the external source.

PWM Control

The ZT7121 is a constant frequency peak-current-mode control PWM switching regulator. Refer to the functional block diagram. The high side N-Channel DMOS power switch turns on at the beginning of each clock cycle. The current in the inductor increases until the PWM current comparator trips to turn off the high side DMOS switch. The peak inductor current at which the current comparator shuts off the high side power switch is controlled by the COMP voltage at the output of feedback error amplifier. The transconductance from the COMP voltage to the output current is set at 11.25A/V. This current-mode control greatly simplifies the feedback compensation design by approximating the switching converter as a single-pole system. Only Type II compensation network is needed, which is integrated into the ZT7121. The loop bandwidth is adjusted by changing the upper resistor value of the resistor divider at the FB pin. The internal compensation in the ZT7121 simplifies the compensation design, minimizes external component counts, and keeps the flexibility of external compensation for optimal stability and transient response.

Enable and Frequency Synchronization

The EN/SYNC pin is a dual function input. Forcing this pin below 0.4V for longer than 4μs shuts down the part; forcing this pin above 1.6V for longer than 4μs turns on the part. Applying a 1MHz to 2MHz clock signal to this pin also synchronizes the internal oscillator frequency to the external clock. When the external clock is used, the part turns on after detecting the first few clocks regardless of duty cycles. If any ON or OFF period of the clock is longer than 4μs, the signal will be intercepted as an enable input and disables the synchronization.

Soft-Start and Output Pre-Bias Startup

When the soft-start period starts, an internal current source begins charging an internal soft-start capacitor. During soft-start, the voltage on the soft-start capacitor is connected to the non-inverting input of the error amplifier. The soft-start period lasts until the voltage on the soft-start capacitor exceeds the reference voltage of 0.8V. At this point the reference voltage takes over at the non-inverting error amplifier input. The soft-start time is internally set at 120μs. If the output of the ZT7121 is pre-biased to a certain voltage during startup, the IC will disable the switching of both high-side and low-side switches until the voltage on the internal soft-start capacitor exceeds the sensed output voltage at the FB pin.

Over current Protection

The ZT7121 offers cycle-to-cycle current limiting for both high-side and low-side switches. The high-side current

limit is relatively constant regardless of duty cycles. When the output is shorted to ground, causing the output voltage to drop below 70% of its nominal output, the IC is shut down momentarily and begins discharging the soft-start capacitor. It will restart with a full soft-start when the soft-start capacitor is fully discharged. This hiccup process is repeated until the fault is removed.

Power Good Output

The ZT7121 includes an open-drain Power Good output that indicates whether the regulator output is within ±10% of its nominal output. When the output voltage moves outside this range, the POK output is pulled to ground. There is a 30µs deglitch time when the POK output change its state.

Bootstrap

The gate driver for the high-side N-channel DMOS power switch is supplied by a bootstrap capacitor connected between the BS and SW pins. When the low-side switch is on, the capacitor is charged through an internal boost diode. When the low-side switch is off and the high-side switch turns on, the voltage on the bootstrap capacitor is boosted above the input voltage and the internal bootstrap diode prevents the capacitor from discharging.

No external bootstrap diode is required for typical applications. For applications with low input voltage or where output voltage is very close to input voltage, an external Schottky diode may be connected from the IN to BS pins to charge the bootstrapped capacitor more strongly for increased gate drive voltage. When using the external bootstrap diode, a resistor at the regulator output or a minimal load current may be required as the bootstrap capacitor always see the supply voltage even when the part is disabled.

Output Voltage Setting

The external resistor divider sets the output voltage (refer to typical application circuit). The feedback resistor R1 also sets the feedback loop bandwidth with the internal compensation. Choose R1 around 300kΩ for optimal transient response. R2 is then given by:

$$R2 = R1 / (V_{OUT}/0.8V - 1)$$

V_{OUT} (V)	R1 (Ω)	R2 (Ω)
1.2	300k (1%)	604k (1%)
1.5	300k (1%)	340k (1%)
1.8	300k (1%)	240k (1%)
2.5	300k (1%)	140k (1%)

Table 1: Resistor selection vs. output voltage setting.

Inductor Selection

A 0.47µH to 1µH inductor with DC current rating at least 25% higher than the maximum load current is recommended for most applications. For best efficiency, the inductor DC resistance shall be <10mΩ. For most designs, the inductance value can be derived from the following equation:

$$L = V_{OUT} \times (V_{IN} - V_{OUT}) / (V_{IN} \times \Delta I_L \times f_{OSC})$$

where ΔI_L is Inductor Ripple Current. Choose inductor ripple current approximately 30% of the maximum load current.

The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \Delta I_L/2$$

Under light load conditions, larger inductance is recommended for improved efficiency.

Input Capacitor Selection

The input capacitor reduces the surge current drawn from the input and the switching noise from the device. The input capacitor impedance at the switching frequency shall be less than input source impedance to prevent high frequency switching current passing to the input source. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 47µF capacitor is sufficient.

Output Capacitor Selection

The output capacitor keeps output voltage ripple small and ensures a stable regulation loop. The output capacitor impedance shall be low at the switching frequency. Ceramic capacitors with X5R or X7R

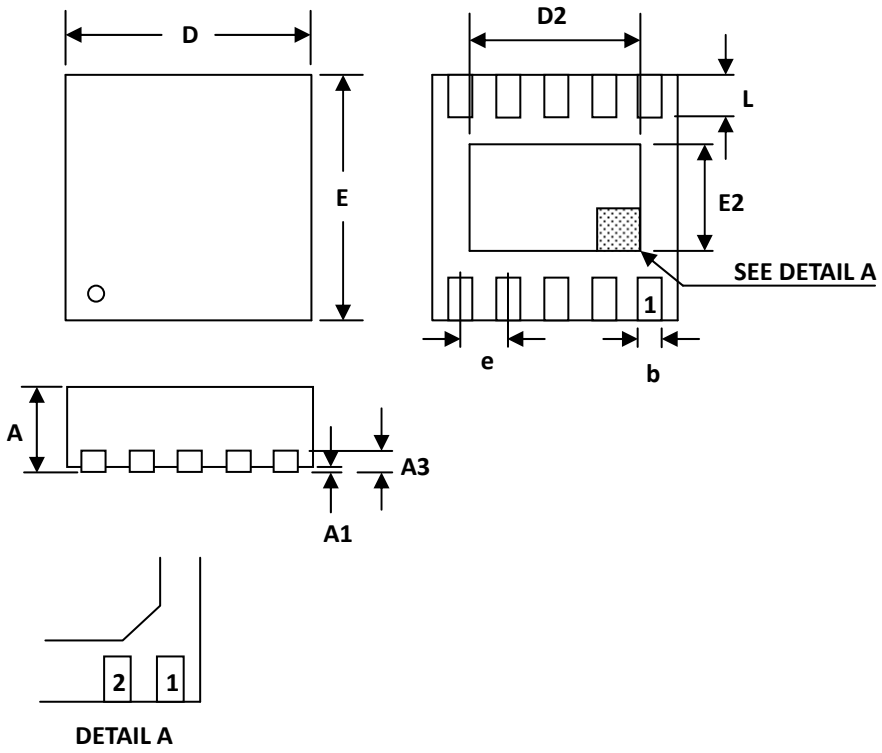
dielectrics are recommended. The output ripple ΔV_{OUT} is approximately:

$$\Delta V_{OUT} \leq \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{OSC} \times L} \times (ESR + \frac{1}{8 \times f_{OSC} \times C3})$$

PCB Layout Considerations

The high current paths (GND, IN and SW) should be placed very close to the device with short, direct and wide traces. Input capacitor C1 needs to be as close as possible to the IN and GND pins. The external feedback resistors shall be placed next to the FB pin. Keep the switching node SW short and away from the feedback network.

PACKAGE DIMENSION DEN 3×3-10L



Symbol	Dimensions in mm		Dimensions in Inch	
	Min	Max	Min	Max
A	0.800	1.000	0.031	0.039
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	2.300	2.650	0.091	0.104
E	2.950	3.050	0.116	0.120
E2	1.500	1.750	0.059	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018